M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
M37267EE-XXXSP, M37267EESP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37267M4-XXXSP, M37267M6-XXXSP and M37267M8-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. They are housed in a 52-pin shrink plastic molded DIP. In addition to their simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming.

The M37267M6-XXXSP has a OSD display function and a data slicer function, so it is useful for a channel selection system for TV with a closed caption decoder. The features of the M37267EE-XXXSP and the M37267EESP are similar to those of the M37267M6-XXXSP except the following: ROM size, RAM size, kinds of character, and that these chips have a built-in PROM which can be written electrically. The difference between M37267M4-XXXSP, M37267M6-XXXSP and the M37267M8-XXXSP are the ROM size and the RAM size as shown below. Accordingly, the following descriptions will be for the M37267M6-XXXSP unless otherwise noted.

Type name	ROM size	RAM size	Kinds of character
M37267M4-XXXSP	16 K bytes	896 bytes	192 kinds
M37267M6-XXXSP	24 K bytes	960 bytes	192 kinds
M37267M8-XXXSP	32 K bytes	1024 bytes	192 kinds
M37267EE-XXXSP	56 K bytes	1536 bytes	256 kinds
M37267EESP	56 K bytes	1536 bytes	256 kinds

FEATURES

- Number of basic instructions 71
- Memory size
  - ROM ..... 16 K bytes (M37267M4-XXXSP)
    24 K bytes (M37267M6-XXXSP)
    32 K bytes (M37267M8-XXXSP)
    56 K bytes (M37267EE-XXXSP, M37267EESP)
  - RAM ..... 896 bytes (M37267M4-XXXSP)
    960 bytes (M37267M6-XXXSP)
    1024 bytes (M37267M8-XXXSP)
    1536 bytes (M37267EE-XXXSP, M37267EESP)
  - ROM for display ..... 3648 bytes
  - RAM for display ..... 272 bytes
- The minimum instruction execution time ..... 0.5μs (at 8 MHz oscillation frequency)
- Power source voltage ..... 5 V ± 10 %
- Subroutine nesting ..... 96 levels (maximum)
- Interrupts ..... 16 types, 15 vectors
- 8-bit timers 6
- Programmable I/O ports (Ports P0, P1, P2, P30, P31) 26
- Input ports (Ports P40–P46, P63, P64) 9
- Output ports (Ports P52–P55) 4
- 12 V withstand ports 7
- LED drive ports 2
- Serial I/O ..... 8-bit × 1 channel
- Multi-master I^2C-BUS interface 1
- A-D comparator (6-bit resolution) ..... 4 channels
- PWM output circuit ..... 8-bit × 7
- Interrupt interval determination circuit
- Power dissipation
  - In high-speed mode 165mW
    (at Vcc = 5.5V, 8MHz oscillation frequency, CRT on, and Data slicer on)
  - In low-speed mode 0.33mW
    (at Vcc = 5.5V, 32kHz oscillation frequency)
- Data slicer
- CRT display function
  - Number of display characters ..... 34 characters × 4 lines (16 lines maximum)
  - Kinds of characters ..... 192 kinds
  - Dot structure ..... CCD mode : 8 × 13 dots
    OSD mode : 8 × 10 dots
    (character part : 8 × 10 dots in both mode)
  - Kinds of character sizes ..... 5 kinds (minimum dot width is 1/2 scanning line)
  - Kinds of character colors (It can be specified by the character) maximum 7 kinds (R, G, B)
  - Kinds of character background colors (It can be specified by the screen, switching to character color is possible.) maximum 7 kinds (R, G, B)
  - Kinds of raster colors (maximum 7 kinds)
  - 2 blanking output (OUT1, OUT2)
  - Display position
    - Horizontal ..... 128 levels
    - Vertical ..... 512 levels
  - Simultaneos display of caption and channel selection
  - Smooth Roll-up
  - Mixing
  - Text display ..... 15 lines

APPLICATION

TV included a closed caption decoder

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
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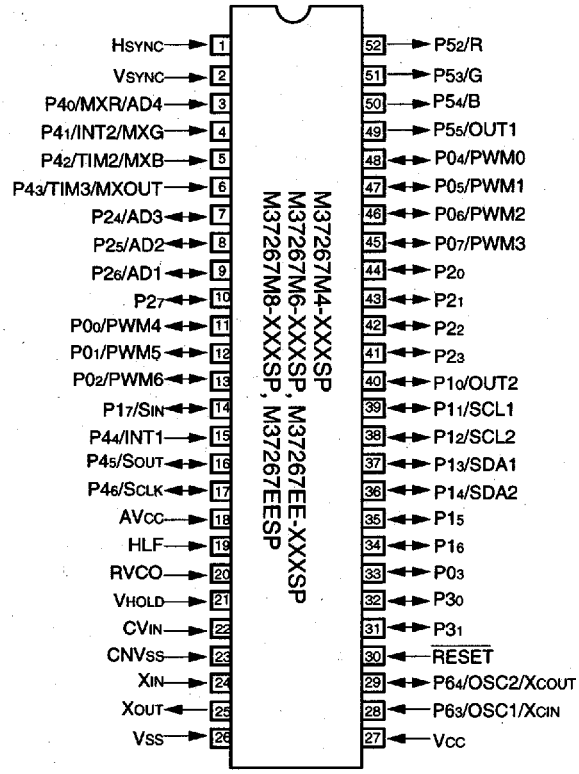
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
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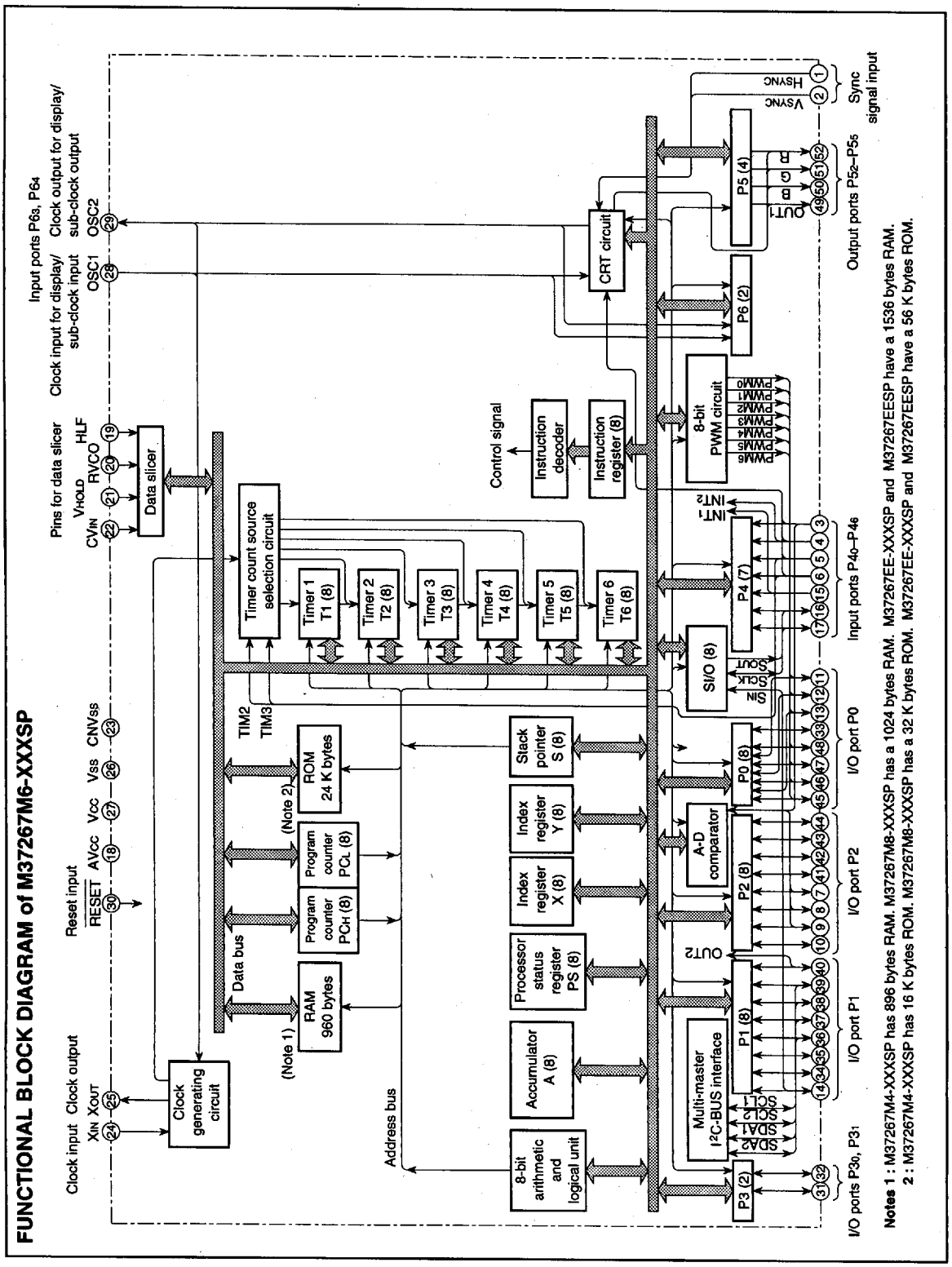
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

FUNCTIONAL BLOCK DIAGRAM of M37267M6-XXXSP



Notes 1 : M37267M4-XXXSP has 896 bytes RAM. M37267M8-XXXSP has a 1024 bytes RAM. M37267EE-XXXSP and M37267EESP have a 1536 bytes RAM.
2 : M37267M4-XXXSP has 16 K bytes ROM. M37267M8-XXXSP has a 32 K bytes ROM. M37267EE-XXXSP and M37267EESP have a 56 K bytes ROM.

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

FUNCTIONS

Parameter			Functions
Number of basic instructions			71
Instruction execution time			0.5 μs (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency			8 MHz (maximum)
Memory size	ROM		24 K bytes
	RAM		960 bytes
	CRT ROM		3648 bytes
	CRT RAM		272 bytes
Input/Output ports	P00–P02, P04–P07	I/O	7-bit × 1 (N-channel open-drain output structure, can be used as PWM output pins)
	P03	I/O	1-bit × 1 (CMOS input/output structure)
	P10, P15–P17	I/O	4-bit × 1 (CMOS input/output structure, can be used as CRT output pin, serial input pin)
	P11–P14	I/O	4-bit × 1 (N-channel open-drain output structure, can be used as multi-master I^2C-BUS interface)
	P2	I/O	8-bit × 1 (CMOS input/output structure, can be used as A-D input pins)
	P30, P31	I/O	2-bit × 1 (CMOS input/output structure)
	P40–P44	Input	5-bit × 1 (can be used as A-D input pins, mixing input pins, INT input pins, external clock input pins)
	P45, P46	Input	2-bit × 1 (N-channel open-drain output structure when serial I/O is used, can be used as serial I/O pins)
	P52–P55	Output	4-bit × 1 (CMOS output structure, can be used as CRT output pins)
	P63	Input	1-bit × 1 (can be used as sub-clock input pin, CRT display clock input pin)
	P64	Input	1-bit × 1 (CMOS output structure when LC is oscillating, can be used as sub-clock output pin, CRT display clock output pin)
Serial I/O			8-bit × 1
Multi-master I^2C-BUS interface			1
A-D comparator			4 channels (6-bit resolution)
PWM output circuit			8-bit × 7
Timers			8-bit timer × 6
Subroutine nesting			96 levels (maximum)
Interrupt interval determination circuit			1
Interrupt			External interrupt × 2, Internal timer interrupt × 5, Serial I/O interrupt × 1, CRT interrupt × 1, Multi-master I^2C-BUS interface interrupt × 1, f(XIN)/4096 interrupt × 1, VSYNC interrupt × 1, BRK interrupt × 1
Clock generating circuit			2 built-in circuits (externally connected a ceramic resonator or a quartz-crystal oscillator)

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FUNCTIONS (continued)

Parameter				Functions
Data slicer				Built in
Power source voltage				5 V ± 10 %
Power dissipation	In high-speed mode	CRT ON	Data slicer ON	165 mW typ. (at oscillation frequency f_{CPU} = 8 MHz, f_{CRT} = 13 MHz)
		CRT OFF	Data slicer OFF	82.5 mW typ. (at oscillation frequency f_{CPU} = 8 MHz)
	In low-speed mode	CRT OFF	Data slicer OFF	0.33mW typ. (at oscillation frequency f_{CLK} = 32 kHz, f(XIN) = stopped)
	In stop mode			0.055 mW (maximum)
Operating temperature range				−10 °C to 70 °C
Device structure				CMOS silicon gate process
Package				52-pin shrink plastic molded DIP
CRT display function	Number of display characters			34 characters × 4 lines (maximum 16 lines by software)
	Dot structure			8 × 13 dots (character part : 8 × 10 dots)
	Kinds of characters			192 kinds
	Kinds of character sizes			5 kinds
	Kinds of character colors			Maximum 7 kinds (R, G, B); can be specified by the character
	Display position (horizontal, vertical)			128 levels (horizontal) × 512 levels (vertical)

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

PIN DESCRIPTION

Pin	Name	Input/ Output	Name
VCC, AVCC, VSS.	Power source		Apply voltage of 5 V ± 10 % (typical) to VCC and AVCC, and 0 V to VSS.
CNVSS	CNVSS		This is connected to VSS.
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2 μs or more (under normal VCC conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
XIN	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins XIN and XOUT. If an external clock is used, the clock source should be connected to the XIN pin and the XOUT pin should be left open.
XOUT	Clock output	Output	
P00/PWM4–P02/PWM6, P03, P04/PWM0–P07/PWM3	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure of P03 is CMOS output, that of P00–P02 and P04–P07 are N-channel open-drain output. The note out of this Table gives a full of port P0 function.
	PWM output	Output	Pins P00–P02 and P04–P07 are also used as PWM output pins PWM4–PWM6 and PWM0–PWM3 respectively. The output structure is N-channel open-drain output.
P10/OUT2, P11/SCL1, P12/SCL2, P13/SDA1, P14/SDA2, P15, P16, P17/SIN	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure of P10 and P15–P17 is CMOS output, that of P11–P14 is N-channel open-drain output.
	CRT output	Output	Pins P10 is also used as CRT output pins OUT2. The output structure is CMOS output.
	Multi-master I^2C-BUS interface	Output	Pins P11–P14 are used as SCL1, SCL2, SDA1 and SDA2 respectively, when multi-master I^2C-BUS interface is used. The output structure is N-channel open-drain output.
	Serial I/O data input	Input	P17 pin is also used as serial I/O data input pin SIN.
P20–P23 P24/AD3–P26/AD1, P27	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
	Analog input	Input	Pins P24–P26 are also used as analog input pins AD3–AD1 respectively.
P30, P31	I/O port P3	I/O	Ports P30 and P31 are a 2-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output.
P40/MXR/AD4, P41/INT2/MXG, P42/TIM2/MXB, P43/TIM3/MXOUT, P44/INT1, P45/SOUT, P46/SCLK,	Input port P4	Input	Ports P40–P46 are a 7-bit input port and has basically the same functions as port P0.
	Video signal input for CRT display	Input	Ports P40–P43 are also used as video signal input pins for mixing, MXR, MXB, MXOUT respectively.
	Analog input	Input	P40 pin is also used as analog input pin AD4.
	External interrupt input	Input	Pins P41, P44 are also used as external interrupt input INT2, INT1.
	External clock input	Input	Pins P42 and P43 are also used as external clock input pins TIM2, TIM3 respectively.
	Serial I/O data output	Output	P45 pin is used as serial I/O data output pin SOUT. The output structure is N-channel open-drain output.
	Serial I/O synchronizing clock input/output	I/O	P46 pin is used as serial I/O synchronizing clock input/output pin SCLK. The output structure is N-channel open-drain output.

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SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

PIN DESCRIPTION (continued)

$P5_2$/R, $P5_3$/G, $P5_4$/B, $P5_5$/OUT1	Output port P5	Output	Ports $P5_2$–$P5_5$ are an 4-bit output port and has basically the same functions as port P0. The output structure is CMOS output.
	CRT output	Output	Pins $P5_2$–$P5_5$ are also used as CRT output pins R, G, B, OUT1 respectively. The output structure is CMOS output.
$P6_3$/OSC1/ X_{CIN}, $P6_4$/OSC2/ X_{COUT}	Input port P6	Input	Ports $P6_3$, $P6_4$ are a 2–bit inport and has basically the same functions as port P0.
	Clock input for CRT	Input	$P6_3$ pin is also used as CRT clock input pin OSC1.
	Clock output for CRT	Output	$P6_4$ pin is also used as CRT clock output pin OSC2. The output structure is CMOS output.
	Sub-clock output	Output	$P6_4$ pin is also used as sub-clock output pin X_{COUT}. The output structure is CMOS output.
	Sub-clock input	Input	$P6_3$ pin is also used as sub-clock input pin X_{CIN}.
CV_{IN}	I/O for data slicer	Input	Input composite video signal through a capacitor.
V_{HOLD}		Input	Connect a capacitor between V_{HOLD} and V_{SS}.
RVCO			Connect a resistor between RVCO and V_{SS}.
HLF			Connect a filter using of a capacitor and a resistor between HLF and V_{SS}.
H_{SYNC}	H_{SYNC} input	Input	This is a horizontal synchronizing signal input for OSD.
V_{SYNC}	V_{SYNC} input	Input	This is a vertical synchronizing signal input for OSD.

Note : As shown in the memory map (Figure 3), port P0 is accessed as a memory at address $00C0_{16}$ of zero page. Port P0 has the port P0 direction register (address $00C1_{16}$ of zero page) which can be used to program each bit as an input ("0") or an output ("1"). The pins programmed as "1" in the direction register are output pins. When pins are programmed as "0," they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output "L" voltage has risen, for example, because a light emitting diode was directly driven. The input pins are in the floating state, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37267M6-XXXSP uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instruction can be used.

CPU Mode Register

The CPU mode register contains the stack page selection bit and internal system clock selection bit. The CPU mode register is allocated at address 00FB16.

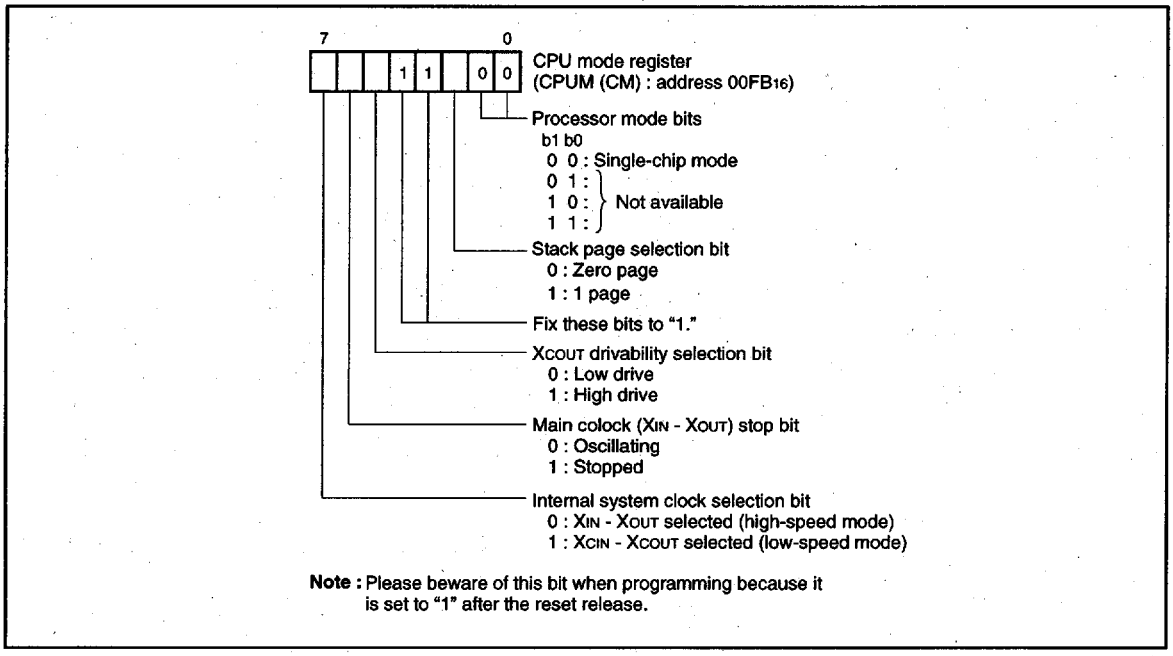

Fig. 1. Structure of CPU mode register

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MEMORY

Special Function Register (SFR) Area
The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM
RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM
ROM is used for storing user programs as well as the interrupt vector area.

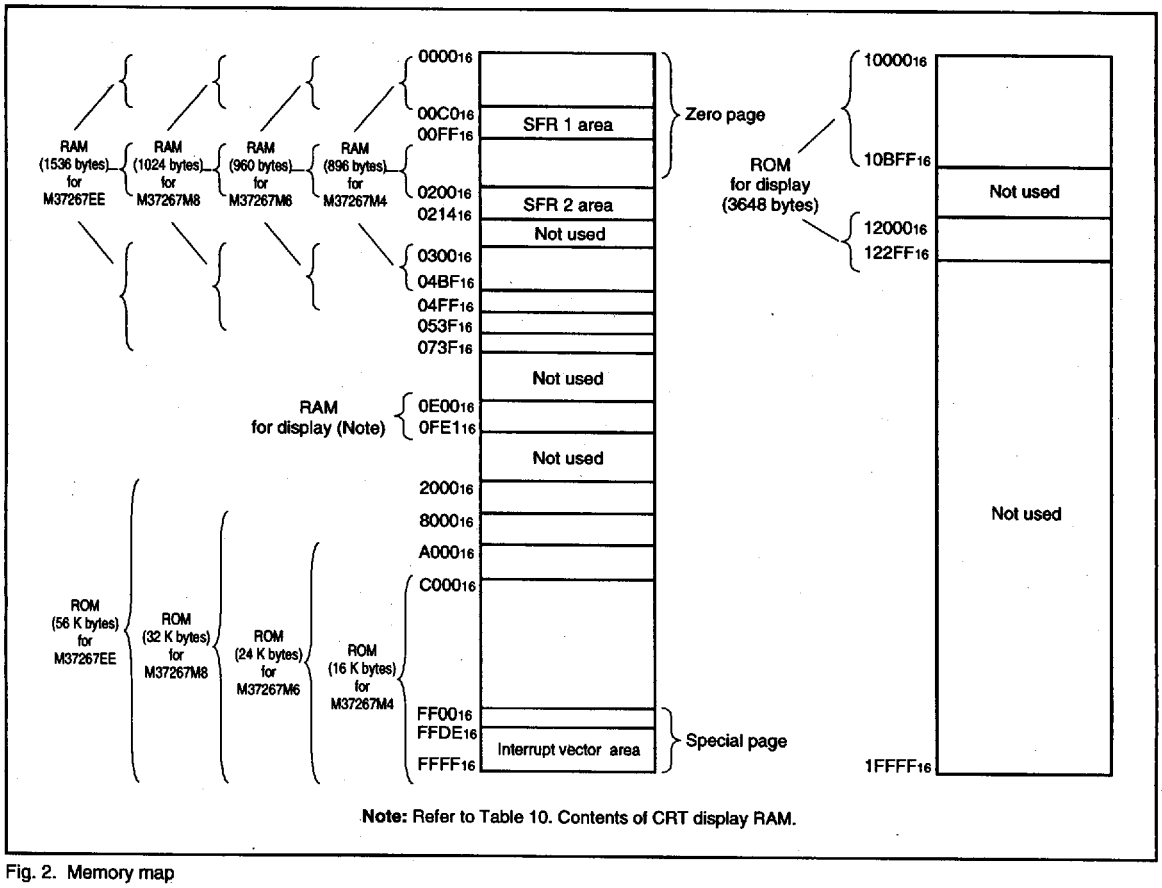
RAM for Display
RAM for display is used for specifying the character codes and colors to display.

ROM for Display
ROM for display is used for storing character data.

Interrupt Vector Area
The interrupt vector area contains reset and interrupt vectors.

Zero Page
The 256 bytes from addresses 000016 to $00FF16$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page
The 256 bytes from addresses $FF0016$ to $FFFF16$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.



Note: Refer to Table 10. Contents of CRT display RAM.

Fig. 2. Memory map

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00C0₁₆	Port P0
00C1₁₆	Port P0 direction register
00C2₁₆	Port P1
00C3₁₆	Port P1 direction register
00C4₁₆	Port P2
00C5₁₆	Port P2 direction register
00C6₁₆	Port P3
00C7₁₆	Port P3 direction register
00C8₁₆	Port P4
00C9₁₆	Port P4 direction register
00CA₁₆	Port P5
00CB₁₆	Port P5 direction register
00CC₁₆	Port P6
00CD₁₆	
00CE₁₆	CRT control register
00CF₁₆	Display mode register
00D0₁₆	Priority display control register
00D1₁₆	Horizontal position register
00D2₁₆	Vertical position register 1
00D3₁₆	Vertical position register 2
00D4₁₆	Vertical position register 3
00D5₁₆	Vertical position register 4
00D6₁₆	Vertical position register 5
00D7₁₆	Character size register 1
00D8₁₆	Character size register 2
00D9₁₆	Display clock selection register 1
00DA₁₆	Display clock selection register 2
00DB₁₆	Background color control register
00DC₁₆	Mask mode register 1
00DD₁₆	Mask mode register 2
00DE₁₆	Data slicer control register 1
00DF₁₆	Data slicer control register 2

00E0₁₆	Caption position register
00E1₁₆	Start bit position register
00E2₁₆	Window register
00E3₁₆	Sync slice register
00E4₁₆	Data register 1
00E5₁₆	Data register 2
00E6₁₆	Clock run-in register 1
00E7₁₆	Clock run-in register 2
00E8₁₆	Clock run-in detect register 1
00E9₁₆	Clock run-in detect register 2
00EA₁₆	Sync pulse counter register
00EB₁₆	Serial I/O mode register
00EC₁₆	Serial I/O register
00ED₁₆	A-D control register 1
00EE₁₆	Interrupt interval determination register
00EF₁₆	Interrupt interval determination control register
00F0₁₆	Timer 1
00F1₁₆	Timer 2
00F2₁₆	Timer 3
00F3₁₆	Timer 4
00F4₁₆	Timer mode register 1
00F5₁₆	Timer mode register 2
00F6₁₆	I²C data shift register
00F7₁₆	I²C address register
00F8₁₆	I²C status register
00F9₁₆	I²C control register
00FA₁₆	I²C clock control register
00FB₁₆	CPU mode register
00FC₁₆	Interrupt request register 1
00FD₁₆	Interrupt request register 2
00FE₁₆	Interrupt control register 1
00FF₁₆	Interrupt control register 2

Fig. 3. Memory map of special function register 1 (SFR 1)

0200₁₆	PWM0 register
0201₁₆	PWM1 register
0202₁₆	PWM2 register
0203₁₆	PWM3 register
0204₁₆	PWM4 register
0205₁₆	PWM5 register
0206₁₆	PWM6 register
0207₁₆	
0208₁₆	
0209₁₆	
020A₁₆	PWM mode register 1
020B₁₆	PWM mode register 2
020C₁₆	Timer 5
020D₁₆	Timer 6
020E₁₆	
020F₁₆	Timer 3 count select register
0210₁₆	OUT control register
0211₁₆	CRT input polarity register
0212₁₆	CRT output control register
0213₁₆	Mixing control register
0214₁₆	A-D control register 2
0215₁₆	
0216₁₆	
0217₁₆	
0218₁₆	
0219₁₆	
021A₁₆	
021B₁₆	
021C₁₆	
021D₁₆	
021E₁₆	
021F₁₆	

Note: Set "00₁₆" to address 020E₁₆.

Fig. 4. Memory map of special function register 2 (SFR 2)

INTERRUPTS

Interrupts can be caused by 16 different sources consisting of 3 external, 11 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted,

(1) The contents of the program counter and processor status register are automatically stored into the stack.
(2) The interrupt disable flag I is set to "1" and the corresponding interrupt request bit is set to "0."
(3) The jump destination address stored in the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to "1."

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 5 shows the structure of the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1," interrupt request bit is "1," and the interrupt disable flag is "0." The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to "0" and "1" by a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 6 shows interrupt control.

Interrupt Causes

(1) VSYNC and CRT interrupts
The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.
The CRT interrupt occurs after character block display to the CRT is completed.

(2) INT1, INT2 interrupts
With an external interrupt input, the system detects that the level of a pin changes from "L" to "H" or from "H" to "L," and generates an interrupt request. The input active edge can be selected by bits 3, 4 and 5 of the interrupt interval determination control register (address 00EF16) : when this bit is "0," a change from "L" to "H" is detected; when it is "1," a change from "H" to "L" is detected. Note that all bits are cleared to "0" at reset.

(3) Timer 1, 2, 3 and 4 interrupts
An interrupt is generated by an overflow of timer 1, 2, 3 or 4.

(4) Serial I/O interrupt
This is an interrupt request from the clock synchronous serial I/O function.

(5) f(XIN)/4096 interrupt
This interrupt occurs regularly with a f(XIN)/4096 period. Set bit 0 of the PWM mode register 1 to "0."

(6) Data slicer interrupt
An interrupt occurs at the end of the line specified in the caption position register.

(7) Multi-master I2C-BUS interface interrupt
This is an interrupt request related to the multi-master I2C-BUS interface.

(8) Timer 5 · 6 interrupt
An interrupt is generated by an overflow of timer 5 or 6. Their priorities are same, and can be switched by software.

(9) BRK instruction interrupt
This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

Table 1. Interrupt vector addresses and priority

Interrupt source	Priority	Vector addresses	Remarks
Reset	1	FFFF16, FFFE16	Non-maskable
CRT interrupt	2	FFFD16, FFFC16	
INT1 interrupt	3	FFFB16, FFFA16	Active edge selectable
Data slicer interrupt	4	FFF916, FFF816	
Serial I/O interrupt	5	FFF716, FFF616	
Timer 4 interrupt	6	FFF516, FFF416	
f(XIN)/4096 interrupt	7	FFF316, FFF216	Active edge selectable
VSYNC interrupt	8	FFF116, FFF016	
Timer 3 interrupt	9	FFEF16, FFEE16	
Timer 2 interrupt	10	FFED16, FFEC16	
Timer 1 interrupt	11	FFEB16, FFEA16	
INT2 interrupt	12	FFE716, FFE616	Active edge selectable
Multi-master I2C-BUS interface interrupt	13	FFE516, FFE416	
Timer 5 · 6 interrupt	14	FFE316, FFE216	
BRK instruction interrupt	15	FFDF16, FFDE16	Non-maskable (software interrupt)

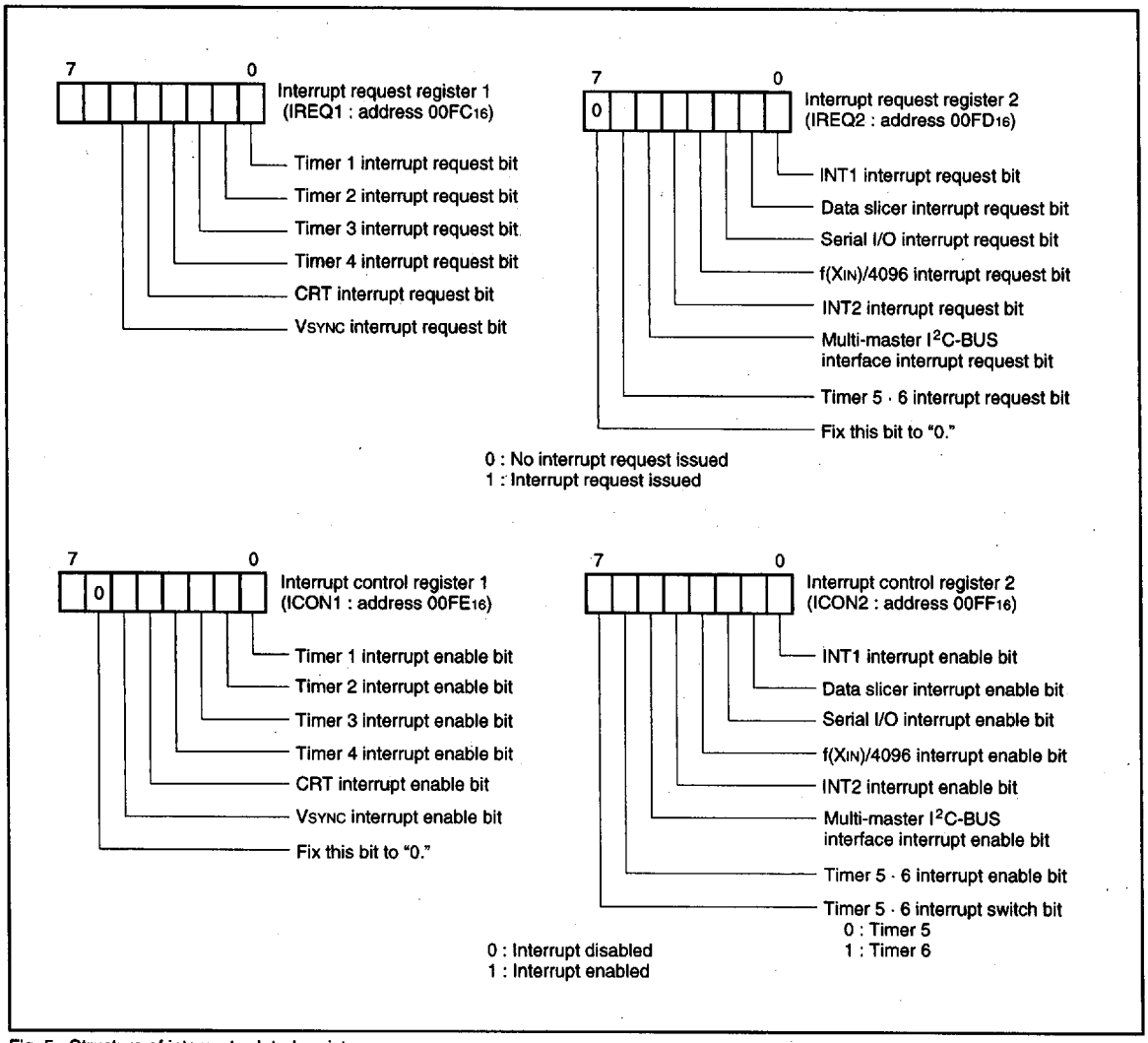


Fig. 5. Structure of interrupt-related registers

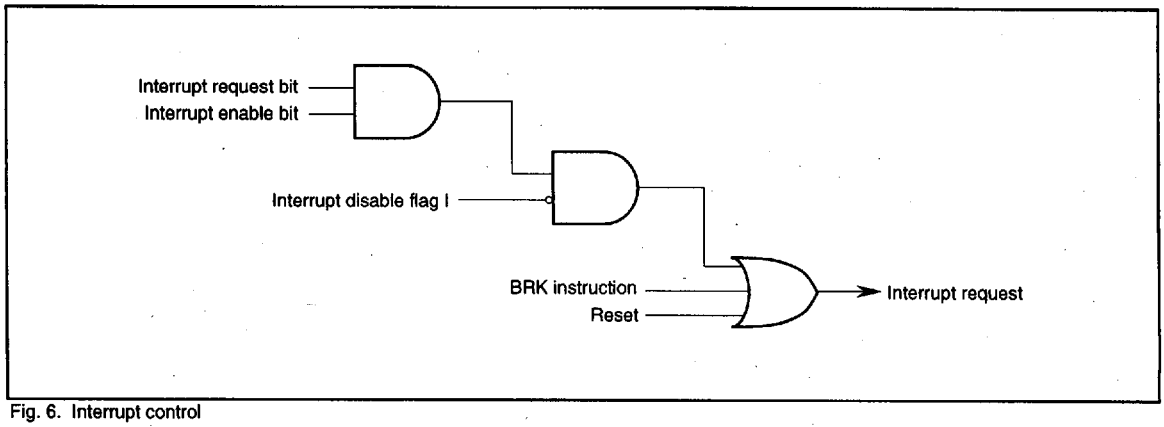


Fig. 6. Interrupt control

TIMERS

The M37267M6-XXXSP has 6 timers: timer 1, timer 2, timer 3, timer 4, timer 5 and timer 6. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 8.

All of the timers count down and their divide ratio is 1/(n+1), where n is the value of timer latch. The value is set to a timer at the same time by writing a count value to the corresponding timer latch (addresses 00F0$_{16}$ to 00F3$_{16}$: timers 1 to 4, addresses 020C$_{16}$ and 020D$_{16}$: timers 5 and 6).

The count value is decremented by 1. The timer interrupt request bit is set to "1" by a timer overflow at the next count pulse after the count value reaches "00$_{16}$".

(1) Timer 1

Timer 1 can select one of the following count sources:

- f(XIN)/16 or f(XCIN)/16
- f(XIN)/4096 or f(XCIN)/4096
- External clock from the P42/TIM2/MXB pin

The count source of timer 1 is selected by setting bits 5 and 0 of the timer mode register 1 (address 00F4$_{16}$). Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

Timer 1 interrupt request occurs at timer 1 overflow.

(2) Timer 2

Timer 2 can select one of the following count sources:

- f(XIN)/16 or f(XCIN)/16
- Timer 1 overflow signal
- External clock from the P42/TIM2/MXB pin

The count source of timer 2 is selected by setting bits 4 and 1 of the timer mode register 1 (address 00F4$_{16}$). Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register. When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

(3) Timer 3

Timer 3 can select one of the following count sources:

- f(XIN)/16 or f(XCIN)/16
- f(XCIN)
- External clock from the P43/TIM3/MXOUT pin

The count source of timer 3 is selected by setting bit 0 of the timer mode register 2 (address 00F5$_{16}$) and bit 0 at address 020F$_{16}$. Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

Timer 3 interrupt request occurs at timer 3 overflow.

(4) Timer 4

Timer 4 can select one of the following count sources:

- f(XIN)/16 or f(XCIN)/16
- f(XIN)/2 or f(XCIN)/2
- f(XCIN)

The count source of timer 3 is selected by setting bits 4 and 1 of the timer mode register 2 (address 00F5$_{16}$). Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register. When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

(5) Timer 5

Timer 5 can select one of the following count sources:

- f(XIN)/16 or f(XCIN)/16
- Timer 2 overflow signal
- Timer 4 overflow signal

The count source of timer 3 is selected by setting bit 6 of the timer mode register 1 (address 00F4$_{16}$) and bit 7 of the timer mode register 2 (address 00F5$_{16}$). Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register.

Timer 5 interrupt request occurs at timer 5 overflow.

(6) Timer 6

Timer 6 can select one of the following count sources:

- f(XIN)/16 or f(XCIN)/16
- Timer 5 overflow signal

The count source of timer 6 is selected by setting bit 7 of the timer mode register 1 (address 00F4$_{16}$). Either f(XIN) or f(XCIN) is selected by bit 7 of the CPU mode register. When timer 5 overflow signal is a count source for the timer 6, the timer 5 functions as an 8-bit prescaler.

Timer 6 interrupt request occurs at timer 6 overflow.

At reset, timers 3 and 4 are connected by hardware and "FF$_{16}$" is automatically set in timer 3; "07$_{16}$" in timer 4. The f(XIN) */16 is selected as the timer 3 count source. The internal reset is released by timer 4 overflow at these state, the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF$_{16}$" is automatically set in timer 3; "07$_{16}$" in timer 4. However, the f(XIN) */16 is not selected as the timer 3 count source. So set both bit 0 of the timer mode register 2 (address 00F5$_{16}$) and bit 0 at address 020F$_{16}$ to "0" before the execution of the STP instruction (f(XIN) */16 is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow at these state, the internal clock is connected.

Because of this, the program starts with the stable clock.

* : When bit 7 of the CPU mode register (CM$_7$) is "1," f(XIN) becomes f(XCIN).

The structure of timer-related registers is shown in Figure 7.

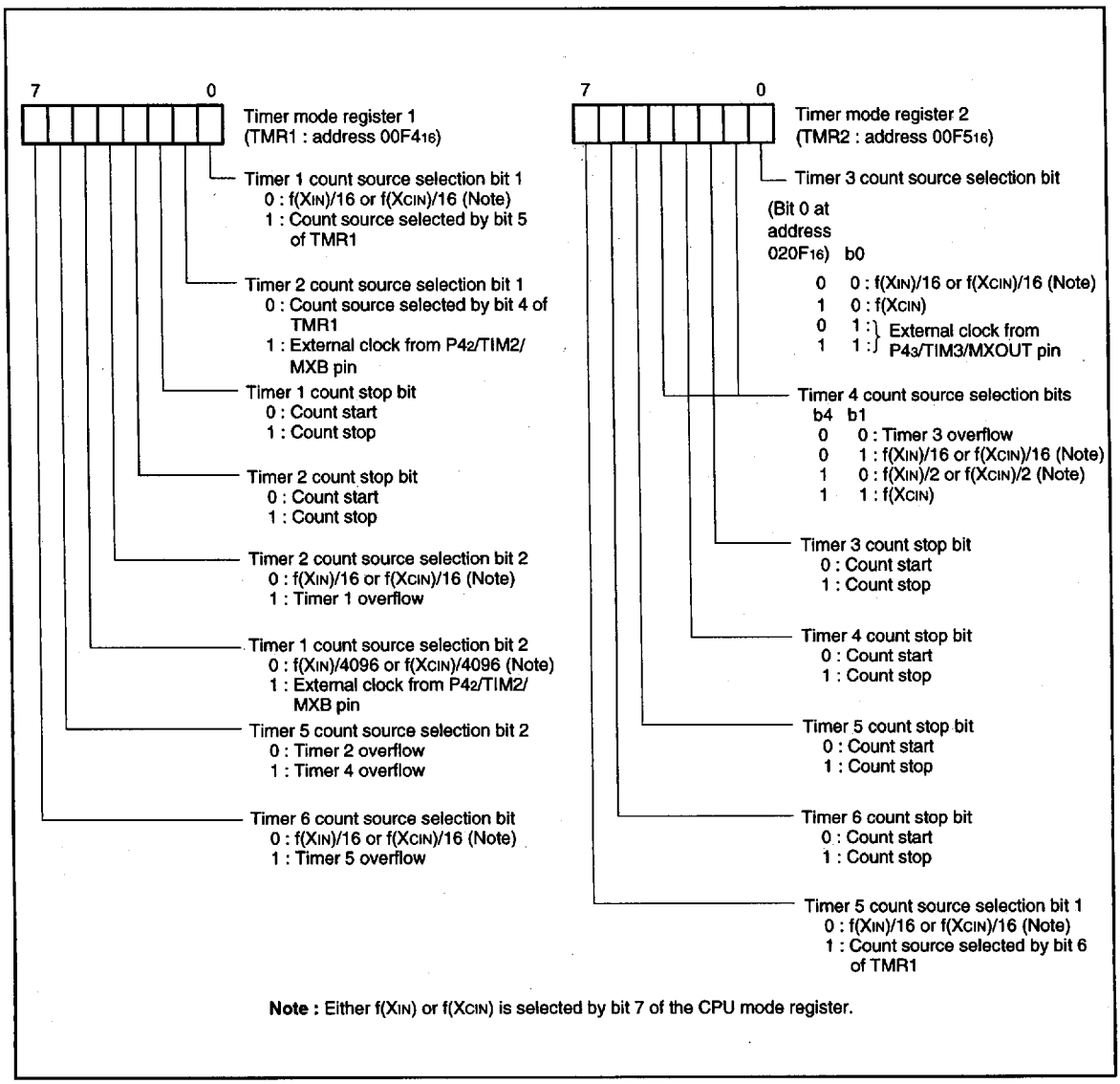
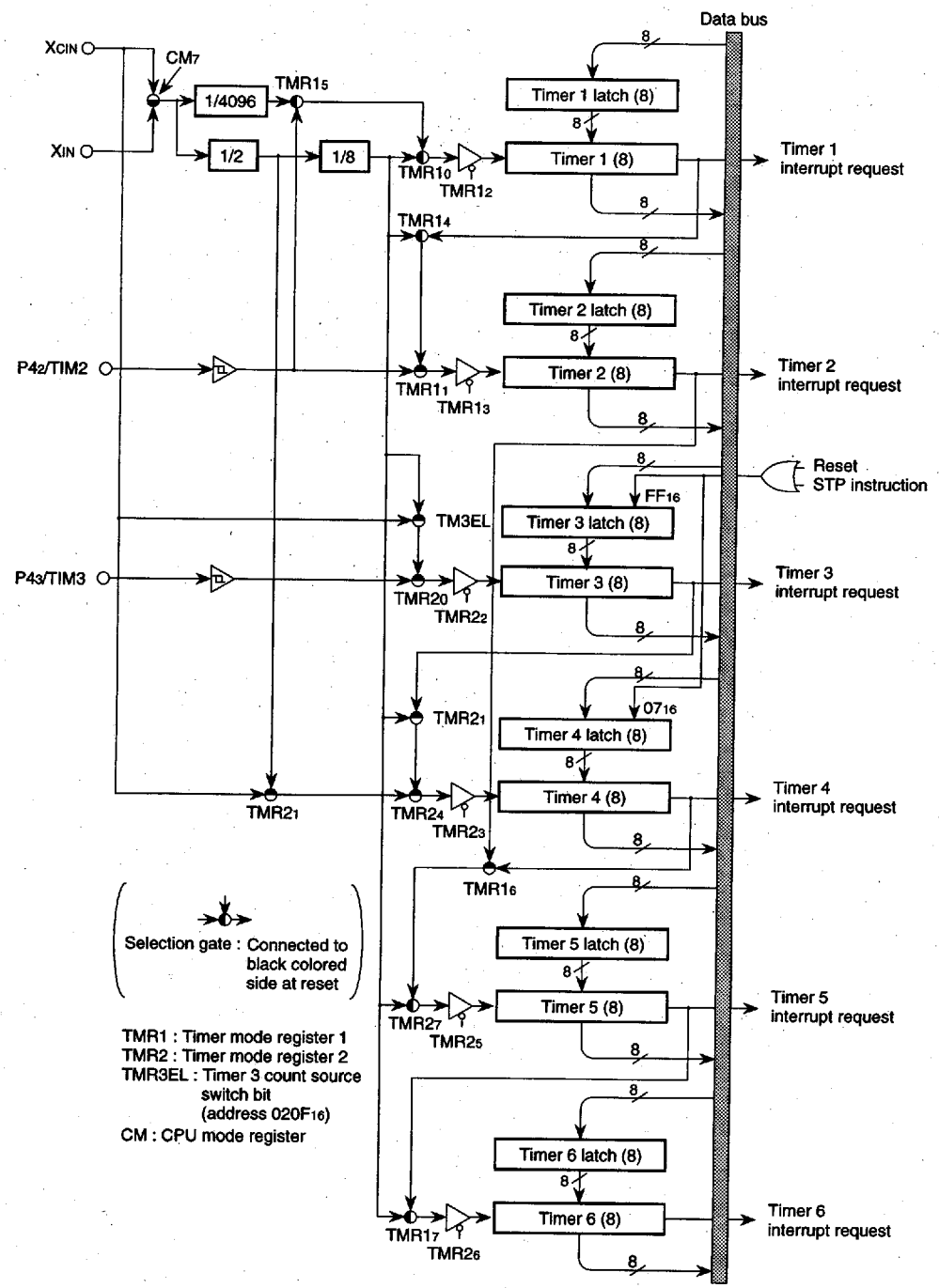


Fig. 7. Structure of timer-related registers



Notes 1: "H" pulse width of external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.
2: When the external clock source is selected, timers 1, 2, and 3 are counted at a rising edge of input signal.
3: In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 8. Timer block diagram

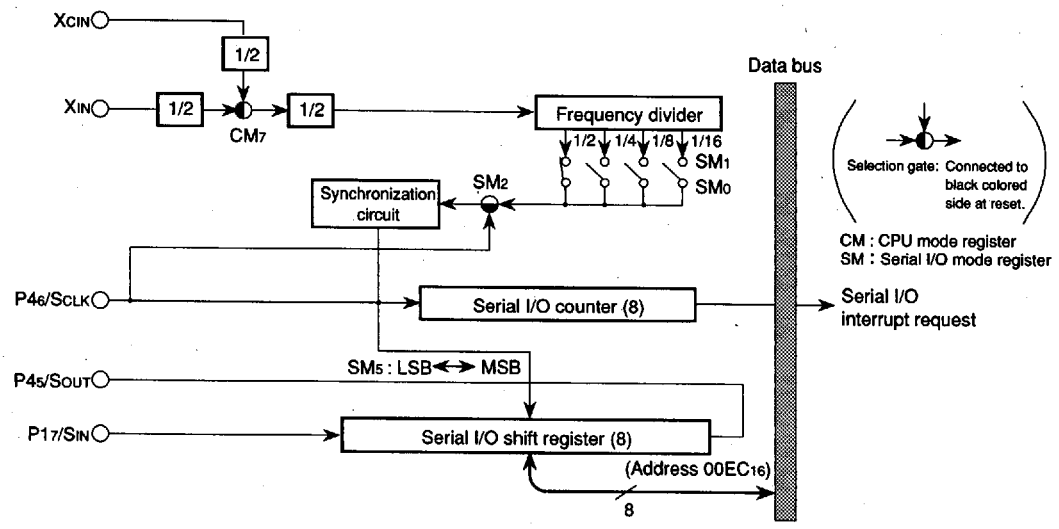
SERIAL I/O

The M37267M6-XXXSP has a built-in serial I/O which can either transmit or receive 8-bit data in serial in the clock synchronous mode.

The serial I/O block diagram is shown in Figure 9. The synchronizing clock I/O pin (SCLK), and data output pin (SOUT) also function as port P4, data input pin (SIN) also functions as port P1.

Bit 2 of the serial I/O mode register (address 00EB16) selects whether the synchronizing clock is supplied internally or externally (from the P46/SCLK pin). When an internal clock is selected, bits 1 and 0 select whether f(XIN) is divided by 8, 16, 32, or 64. To use P45/SOUT and P46/SCLK pins for serial I/O, set the corresponding bits of the port P4 direction register (address 00C916) to "0." To use P17/SIN pin for serial I/O, set the corresponding bit of the port P1 direction register (address 00C316) to "0."

The operation of the serial I/O function is described below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.



Note : When the data is set in the serial I/O register (address 00EC16), the register functions as the serial I/O shift register.

Fig. 9. Serial I/O block diagram

Internal clock—the serial I/O counter is set to "7" during write cycle into the serial I/O register (address 00EC16), and transfer clock goes "H" forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit.

After the transfer clock has counted 8 times, the serial I/O counter becomes "0" and the transfer clock stops at "H." At this time the interrupt request bit is set to "1."

External clock—when an external clock is selected as the clock source, the interrupt request is set to "1" after the transfer clock has counted 8 times. However, transfer operation does not stop, so control the clock externally. Use the external clock of 500kHz or less with a duty cycle of 50%.

The serial I/O timing is shown in Figure 10. When using an external clock for transfer, the external clock must be held at "H" for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

Notes 1: On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions as SEB and CLB instructions.

2: When an external clock is used as the synchronizing clock, write transmit data to the serial I/O register at "H" of the transfer clock input level.

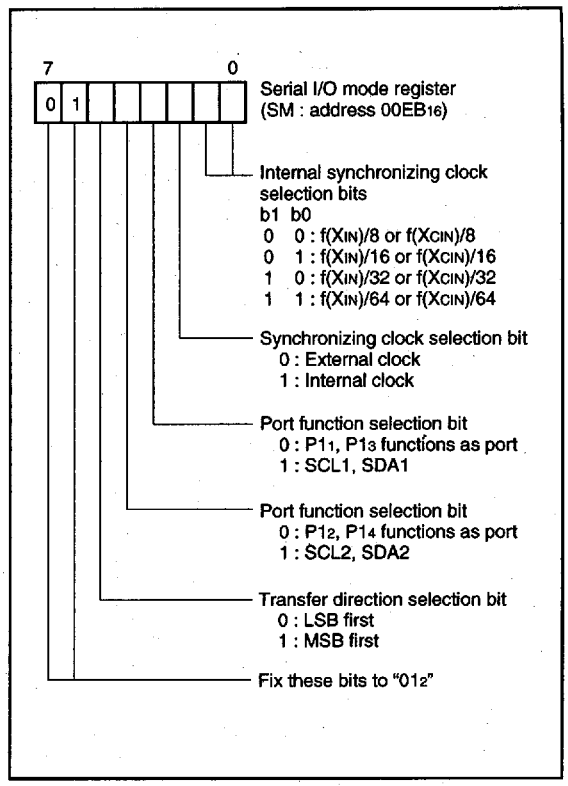
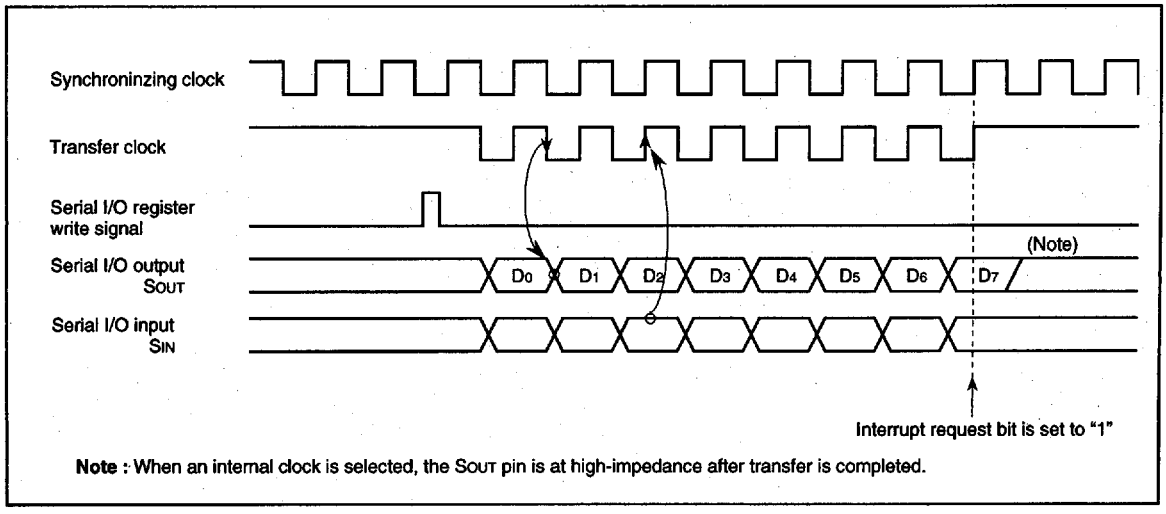


Fig. 11. Structure of serial I/O mode register



Note : When an internal clock is selected, the SOUT pin is at high-impedance after transfer is completed.

Fig. 10. Serial I/O timing (for LSB first)

PWM OUTPUT FUNCTION

The M37267M6-XXXSP is equipped with seven 8-bit PWMs (PWM0–PWM6). PWM0–PWM6 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of 4 μs (for f(XIN) = 8 MHz) and repeat period of 1024 μs.

Figure 12 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to PWM0–PWM6 using f(XIN) divided by 2 as a reference signal.

(1) Data Setting

When outputting PWM0–PWM6, set 8-bit output data in the PWMi register (i means 0 to 6; addresses 020016 to 020616).

(2) Transmitting Data from Register to PWM circuit

Data transfer from the 8-bit PWM register to 8-bit PWM circuit is executed at writing data to the register.

The signal output from the 8-bit PWM output pin corresponds to the contents of this register.

(3) Operating of 8-bit PWM

The following is the explanation about PWM operation.

At first, set the bit 0 of PWM mode register 1 (address $020A16$) to "0" (at reset, bit 0 is already set to "0" automatically), so that the PWM count source is supplied.

PWM0–PWM3 are also used as pins P04–P07, PWM4–PWM6 are also used as pins P00–P02 respectively. Set the corresponding bits of the port P0 direction register to "1" (output mode). And select each output polarity by bit 3 of the PWM mode register 1 (address $020A16$). Then, set bits 6 to 0 of the PWM output control register 2 to "1" (PWM output).

The PWM waveform is output from the PWM output pins by setting these registers.

Figure 13 shows the 8-bit PWM timing. One cycle (T) is composed of 256 (2^8) segments. The 8 kinds of pulses relative to the weight of each bit (bits 0 to 7) are output inside the circuit during 1 cycle. Refer to Figure 13 (a). The 8-bit PWM outputs waveform which is the logical sum (OR) of pulses corresponding to the contents of bits 0 to 7 of the 8-bit PWM register. Several examples are shown in Figure 13 (b). 256 kinds of output ("H" level area: 0/256 to 255/256) are selected by changing the contents of the PWM register. A length of entirely "H" output cannot be output, i.e. 256/256.

(4) Output after Reset

At reset the output of port P00–P02 and P04–P07 is in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
M37267EE-XXXSP, M37267EESP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

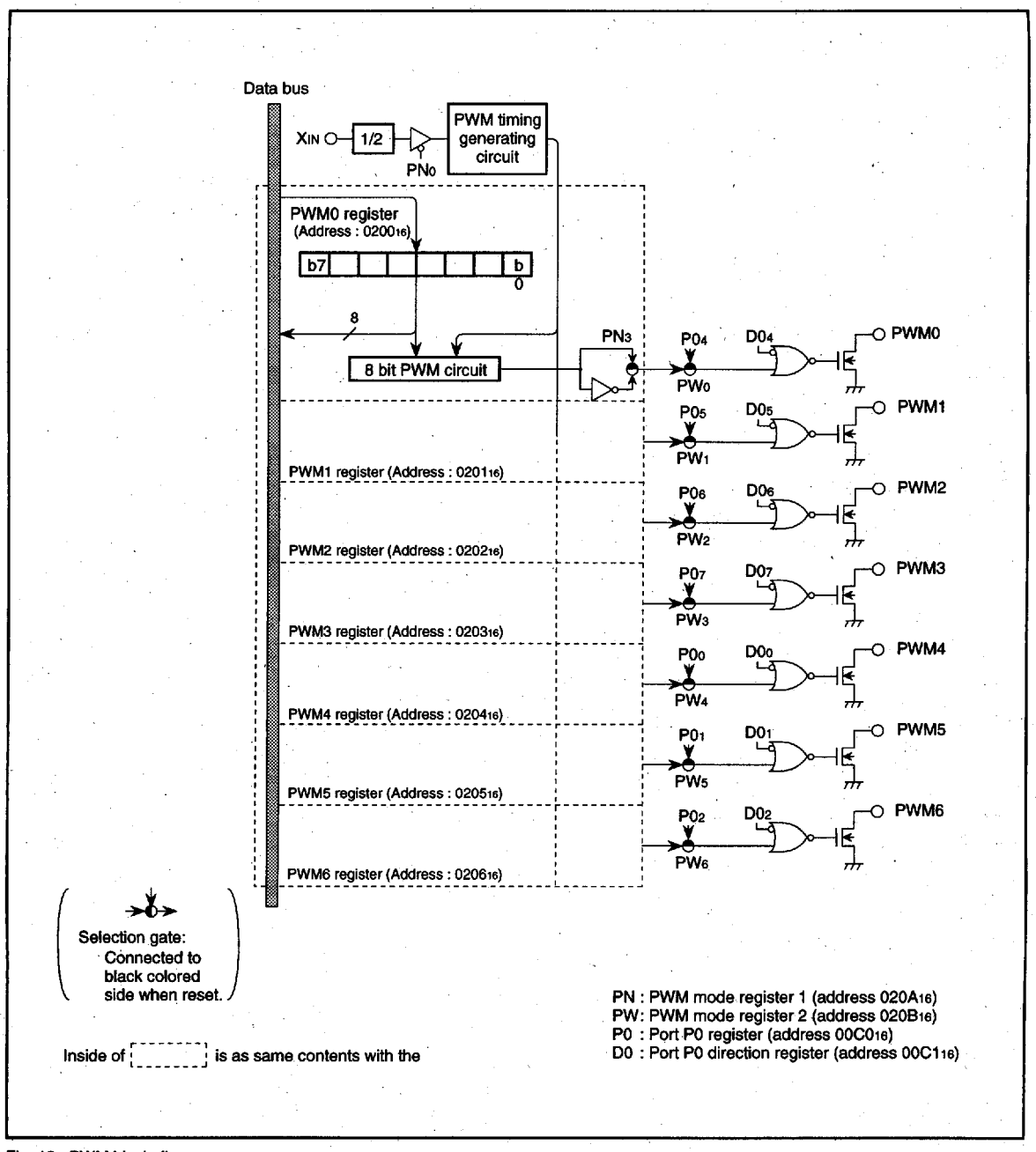


Fig. 12. PWM block diagram

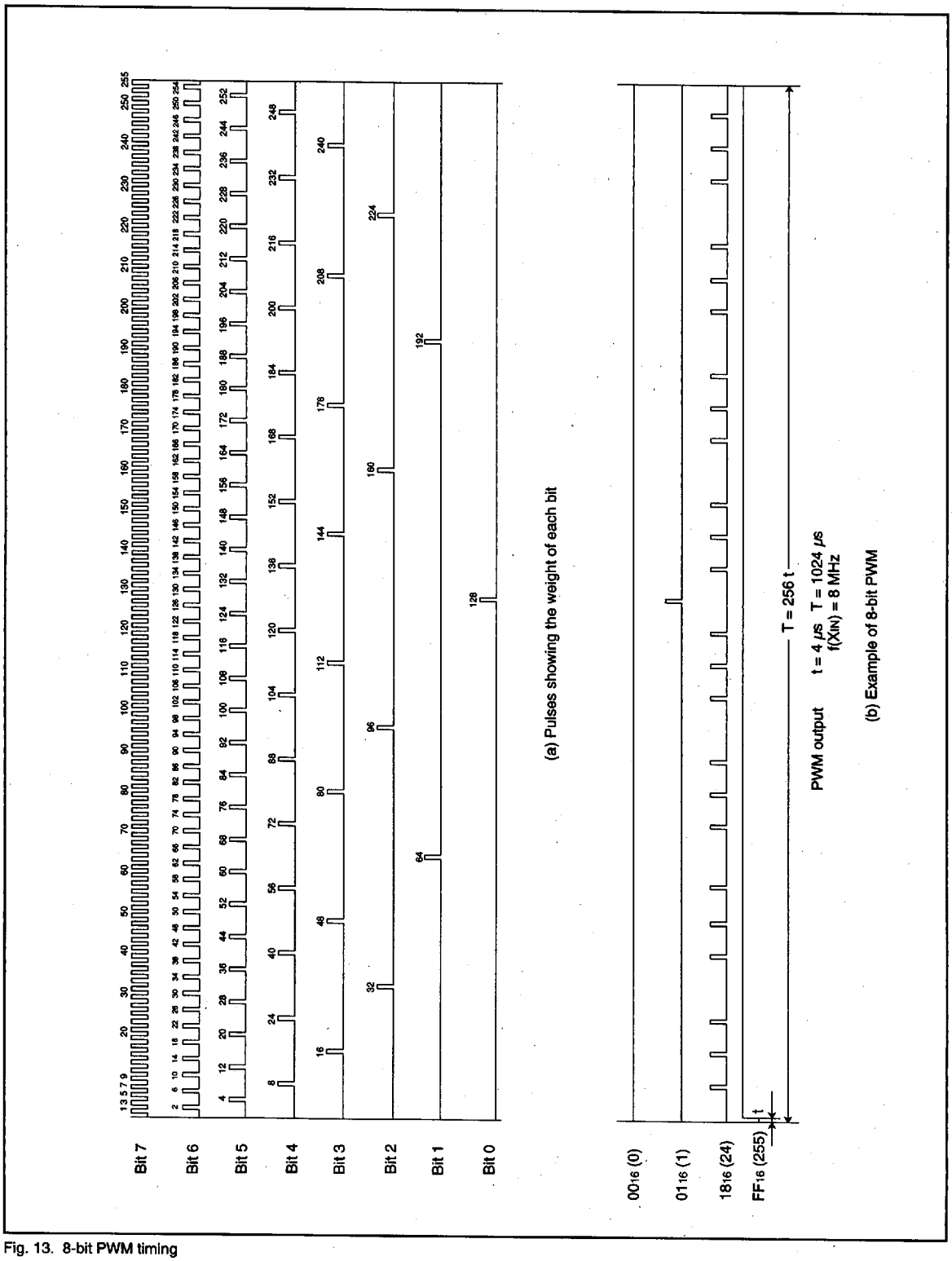


Fig. 13. 8-bit PWM timing

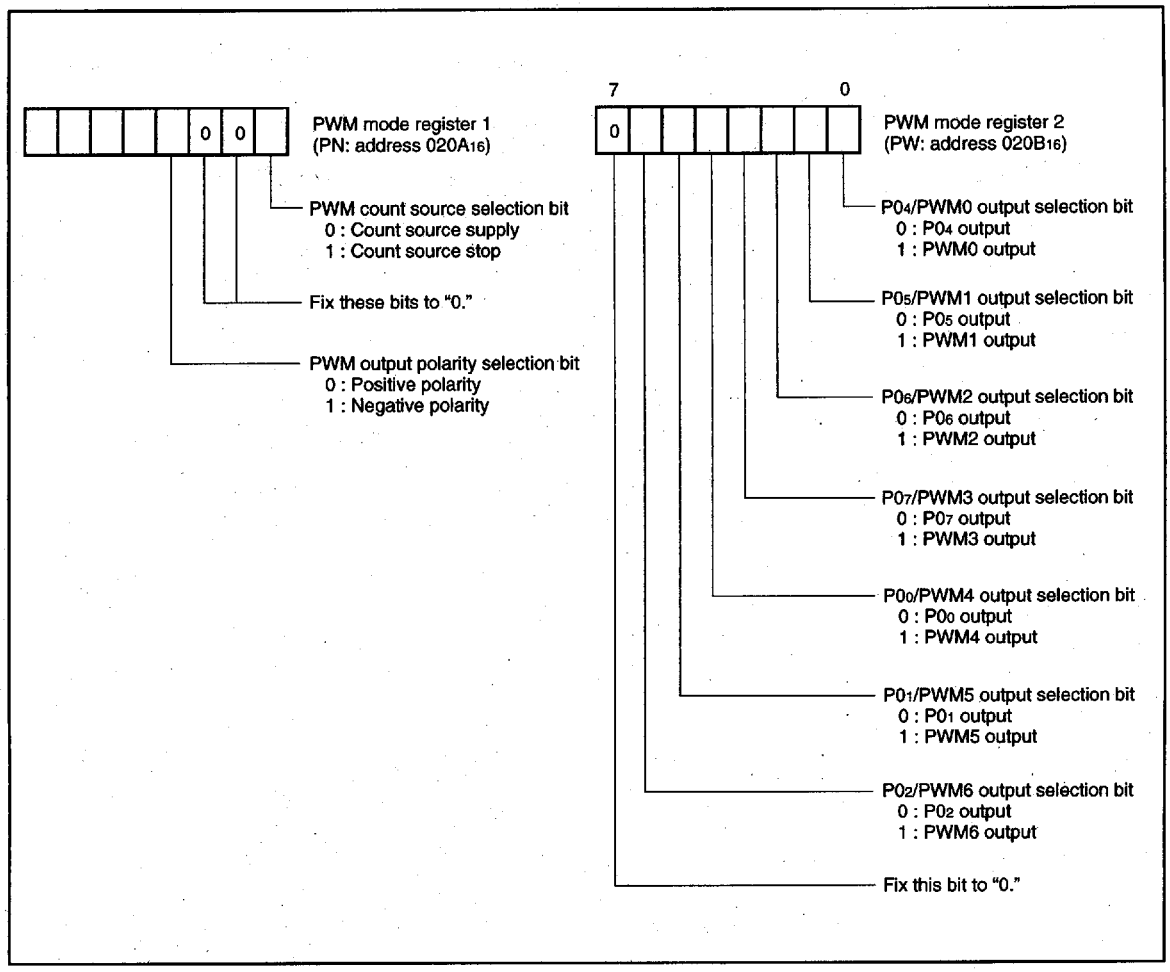


Fig. 14. Structure of PWM-related registers

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
M37267EE-XXXSP, M37267EESP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

A-D COMPARATOR

A-D comparator consists of 6-bit D-A converter and comparator. A-D comparator block diagram is shown in Figure 17.

The reference voltage "V_{ref}" for D-A conversion is set by low-order 5 bits of the A-D control register 1 (address $00ED_{16}$) and bit 0 of the A-D control register 2 (address 0214_{16}).

The comparison result of the analog input voltage and the reference voltage "V_{ref}" is stored in bit 5 of the A-D control register 1.

For A-D comparison, set "0" to corresponding bits of the direction register to use ports as analog input pins. Write the least significant bit of digital value corresponding to V_{ref} to be compared to bit 0 of the A-D control register 2. After that, write the high-order 5 bits of digital value to the low-order 5 bits of the A-D control register 1, and write the data for selecting analog input pins to bits 6 and 7. The voltage comparison starts by writing to the A-D control register 1, and it is completed after 16 machine cycles (NOP instruction × 8).

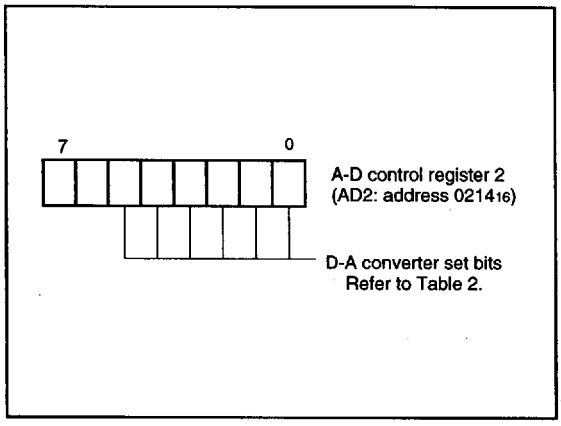


Fig. 16. Structure of A-D control register 1

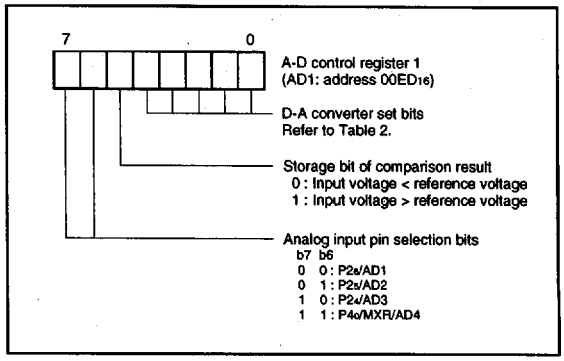


Fig. 15. Structure of A-D control register 2

Table 2. Relation between contents of A-D control registers and reference voltage "V_{ref}"

A-D control register 1					A-D control register 2	Reference voltage "V_{ref}"
Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 0	
0	0	0	0	0	0	1/64 Vcc
0	0	0	0	0	1	2/64 Vcc
0	0	0	0	1	0	3/64 Vcc
0	0	0	0	1	1	4/64 Vcc
0	0	0	1	0	0	5/64 Vcc
0	0	0	1	0	1	6/64 Vcc
⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	0	0	61/64 Vcc
1	1	1	1	0	1	62/64 Vcc
1	1	1	1	1	0	63/64 Vcc
1	1	1	1	1	1	64/64 Vcc

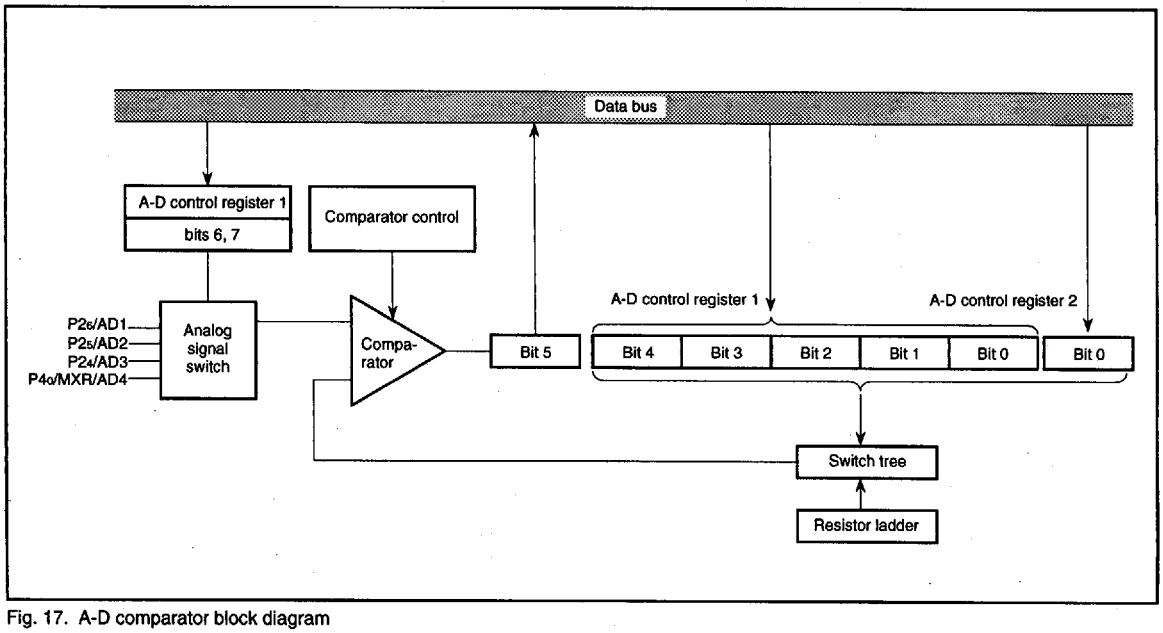


Fig. 17. A-D comparator block diagram

DATA SLICER

The M37267M6-XXXSP includes the data slicer function for the closed caption decoder (referred to as the CCD). This function takes out the caption data superimposed in the vertical blanking interval of a composite video signal. A composite video signal which makes the sync chip's polarity negative is input to the CVIN pin.

When the data slicer function is not used, the data slicer circuit can be cut off by setting bit 0 of the data slicer control register 1 (address $00DE_{16}$) to "0." Also, the timing signal generating circuit can be cut off by setting bit 0 of data slicer control register 2 (address $00DF_{16}$) to "0." These settings can realize the low-power dissipation.

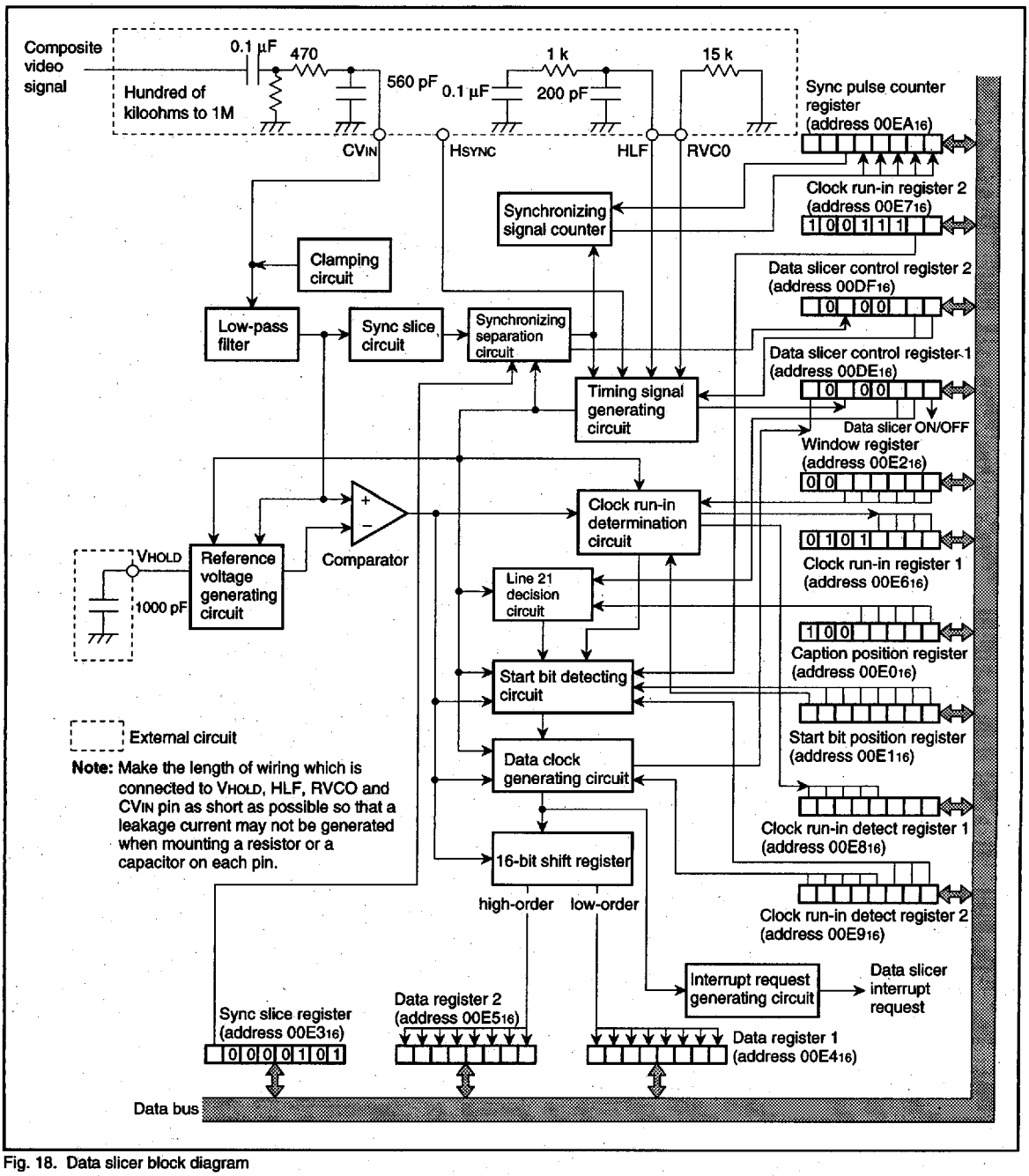


Fig. 18. Data slicer block diagram

Figure 19 shows the structure of the data slicer control register.

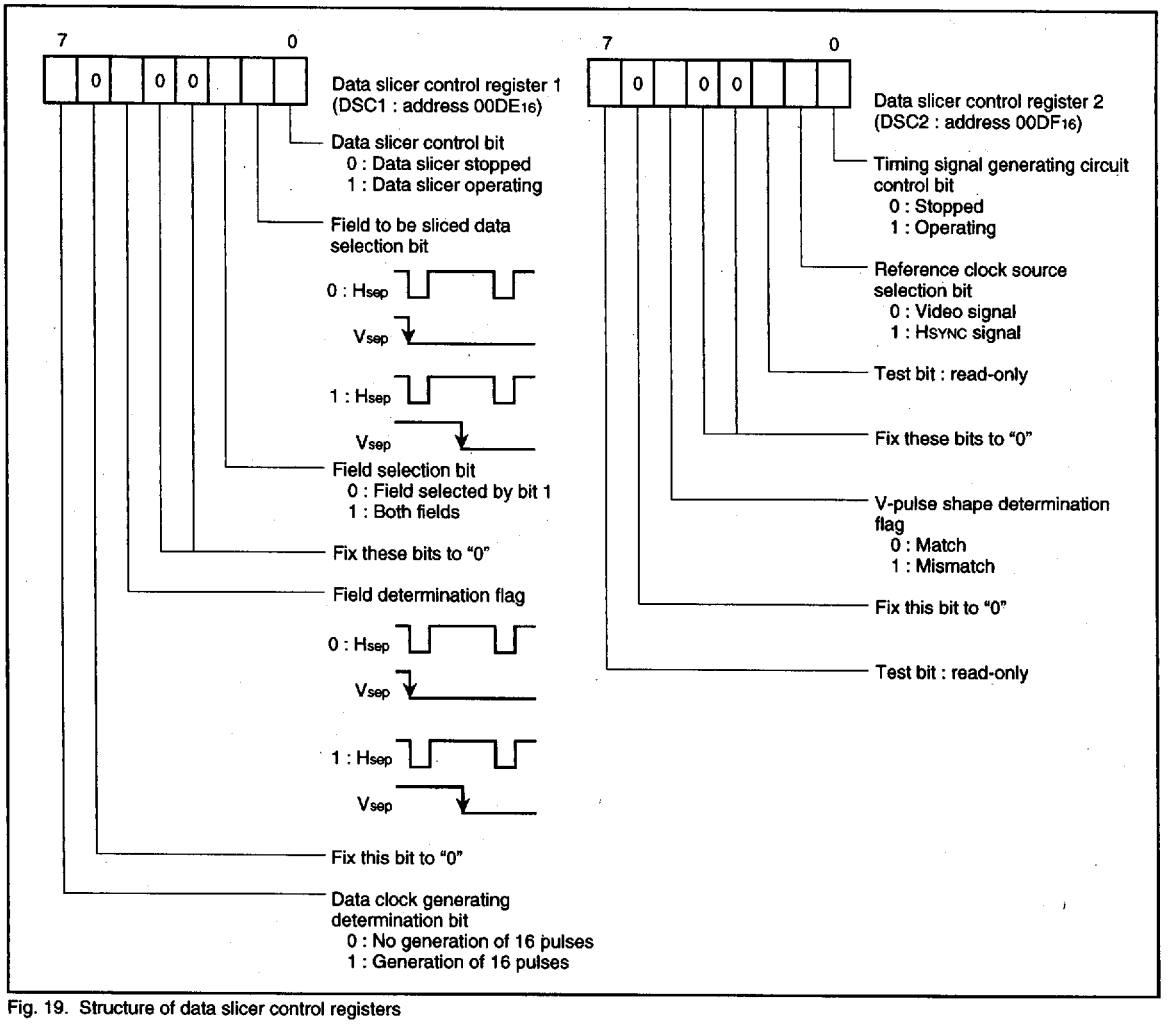


Fig. 19. Structure of data slicer control registers

(1) Clamping Circuit and Low-pass Filter

This filter attenuates the noise of the composite video signal input from the CVIN pin. The CVIN pin to which composite video signal is input requires a capacitor (0.1 μF) coupling outside. Pull down the CVIN pin with a resistor of hundreds of kiloohms to 1 M . In addition, we recommend to install externally a simple low-pass filter using a resistor and a capacitor at the CVIN pin (refer to Figure 18).

(2) Sync Slice Circuit

This circuit takes out a composite sync signal from the output signal of the low-pass filter. Figure 20 shows the structure of the sync slice register.

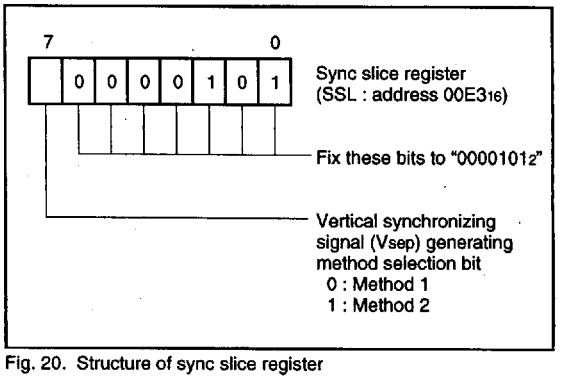


Fig. 20. Structure of sync slice register

(3) Synchronizing Signal Separation Circuit

This circuit separates a horizontal synchronizing signal and a vertical synchronizing signal from the composite sync signal taken out in the sync slice circuit.

① Horizontal synchronizing signal (H_{sep})

A one-shot horizontal synchronizing signal Hsep is generated at the falling edge of the composite sync signal.

② Vertical synchronizing signal (V_{sep})

As a V_{sep} signal generating method, it is possible to select one of the following 2 methods by using bit 7 of the sync slice register (address $00E3_{16}$).

- •Method 1 The "L" level width of the composite sync signal is measured. If this width exceeds a certain time, a V_{sep} signal is generated in synchronization with the rising of the timing signal immediately after this "L" level.
- •Method 2 The "L" level width of the composite sync signal is measured. If this width exceeds a certain time, it is detected whether a falling of the composite sync signal exits or not in the "L" level period of the timing signal immediately after this "L" level. If a falling exists, a V_{sep} signal is generated in synchronization with the rising of the timing signal (refer to Figure 21).

Figure 21 shows a V_{sep} generating timing. The timing signal shown in the figure is generated from the reference clock which the timing generating circuit outputs.

(4) Timing Signal Generating Circuit

This circuit generates a reference clock which is 832 times as large as the horizontal synchronizing signal frequency. It also generates various timing signals on the basis of the reference clock, horizontal synchronizing signal and vertical synchronizing signal. The circuit operates by setting bit 0 of data slicer control register 2 (address $00DF_{16}$) to "1."

The reference clock can be used as a display clock for CRT display function in addition to the data slicer. The HSYNC signal can be used as a count source instead of the composite sync signal. However, when the HSYNC signal is selected, the data slicer cannot be used. A count source of the reference clock can be selected by bit 1 of data slicer control register 2 (address $00DF_{16}$).

Reading bit 5 of data slicer control register 2 permits determinating the shape of the V-pulse portion of the composite sync signal. As shown in Figure 22, when the A level matches the B level, this bit is "0." In the case of a mismatch, the bit is "1."

For the pins RVCO and the HLF, connect a resistor and a capacitor as shown in Figure 18. Make the length of wiring which is connected to these pins as short as possible so that a leakage current may not be generated.

Note: It takes a few tens of milliseconds until the reference clock becomes stable after the data slicer and the timing signal generating circuit are started. In this period, various timing signals, H_{sep} signals and V_{sep} signals become unstable. For this reason, take stabilization time into consideration when programming.

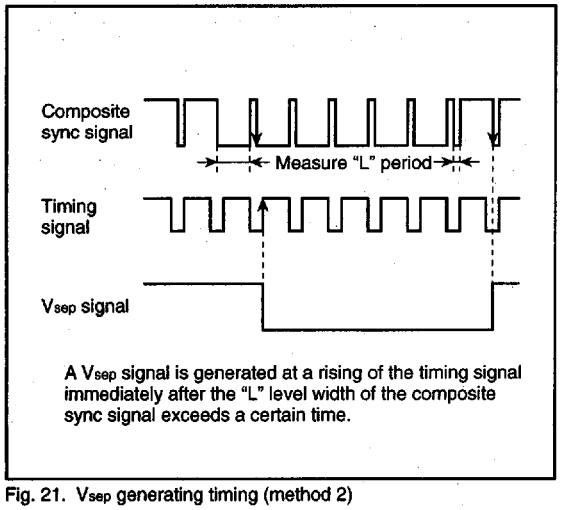


Fig. 21. V_{sep} generating timing (method 2)

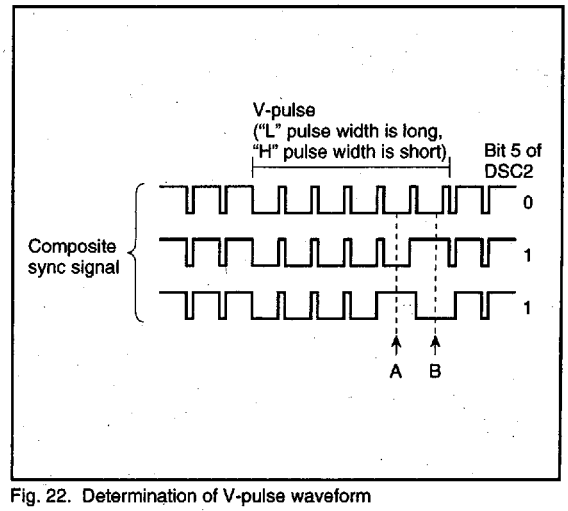


Fig. 22. Determination of V-pulse waveform

(5) Line 21 Decision Circuit

① Decision of line 21

This circuit decides a line (line 21) on which caption data is superimposed.

Set the number of Hsep to be input in the period from a falling of Vsep to a line on which caption data is superimposed in bits 0 to 4 of the caption position register (address $00E0_{16}$). The number of Hsep is counted by hardware. The line which matches the set value in the caption position register is regarded as line 21.

The values of "00_{16}" to "$1F_{16}$" can be set in the caption position register. Bit 7 to bit 5 are used for testing. Set "100_2." Figure 23 shows the signals in the vertical blanking interval. Figure 24 shows the structure of the caption position register.

② Selection of field to be sliced data

Field to be sliced data is selected by bit 1 of data slicer control register 1 (address $00DE_{16}$). When bit 2 of the data slicer control register 1 is set to "1," it is possible to decide line 21 for both fields. The field determination flag can be read out by bit 5 of the data slicer control register 1. This flag changes at the falling of Vsep.

(6) Reference Voltage Generating Circuit and Comparator

The composite video signal clamped by the clamping circuit is input to the reference voltage generating circuit and the comparator.

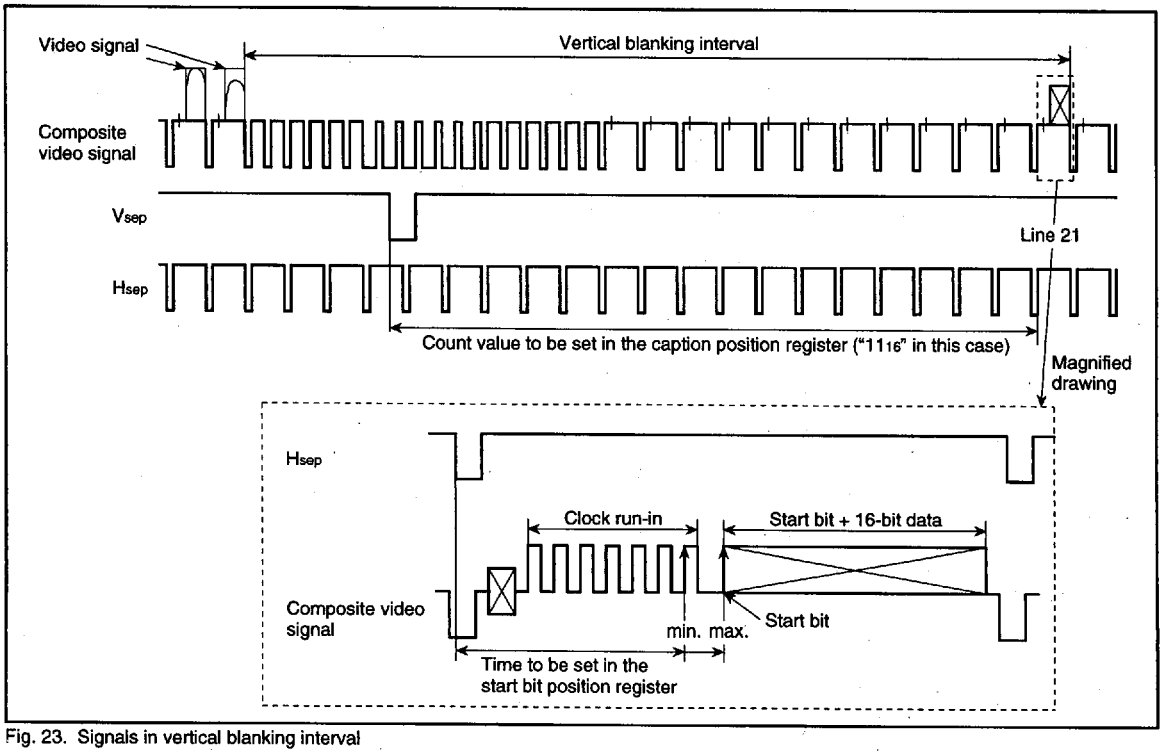


Fig. 23. Signals in vertical blanking interval

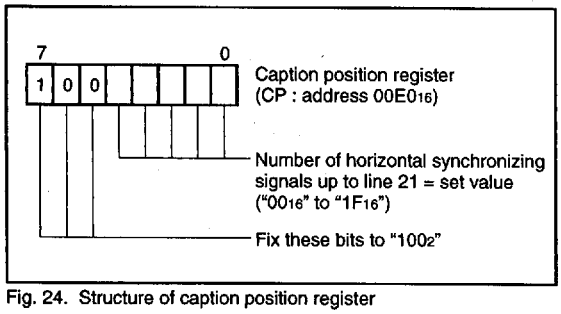


Fig. 24. Structure of caption position register

① Reference voltage generating circuit

This circuit generates a reference voltage (slice voltage) by using the amplitude of the clock run-in at line 21 of the field selected by bit 1 of the data slicer control register. Connect a capacitor of about 1000 pF between the VHOLD pin and the Vss pin, and make the length of wiring as short as possible so that a leakage current may not be generated.

② Comparator

The comparator compares the voltage of the composite video signal with the voltage (reference voltage) generated in the reference voltage generating circuit, and converts the composite video signal into a digital value.

(7) Start Bit Detecting Circuit

This circuit detects a start bit at line 21 decided in the line 21 decision circuit. For start bit detection, it is possible to select one of the following two types by using bit 1 of the clock run-in register 2 (address $00E7_{16}$).

① After the lapse of the time corresponding to the set value of the start bit position register (address $00E1_{16}$), the first rising of the composite video signal is detected as a start bit.

The time is set in bits 0 to 6 of the start bit position register (address $00E1_{16}$) (refer to Figure 26). Set a value fit for the following conditions.

Figure 26 shows the structure of the start bit position register.

[Time from the falling of the horizontal synchronizing signal to the last rising of the clock run-in] < [4 × set value of the start bit position register × reference clock period] < [Time from the falling of the horizontal synchronizing signal to occurrence of the start bit]

② After a falling of the clock run-in pulse set in bits 2 to 0 of clock run-in detect register 2 (address $00E9_{16}$) is detected, a start bit is detected by sampling a comparator output. A sampling clock for sampling is obtained by dividing the reference clock generated in the timing signal generating circuit by 13.

Figure 27 shows the structure of clock run-in detect register 2.

The contents of bits 2 to 0 of clock run-in detect register 2 and bit 1 of clock run-in register 2 are written at a falling of the horizontal synchronizing signal. For this reason, even if an instruction for setting is executed, the contents of the register cannot be rewritten until a falling of the horizontal synchronizing signal.

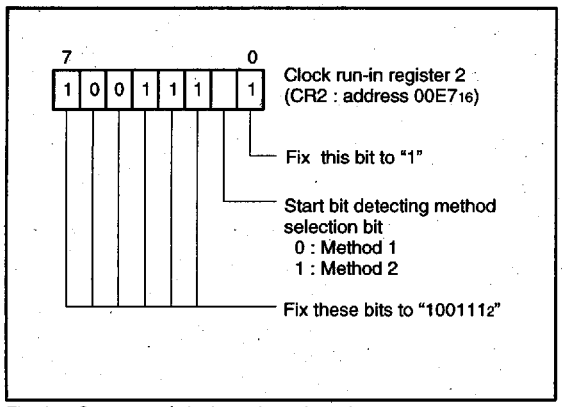


Fig. 25. Structure of clock run-in register 2

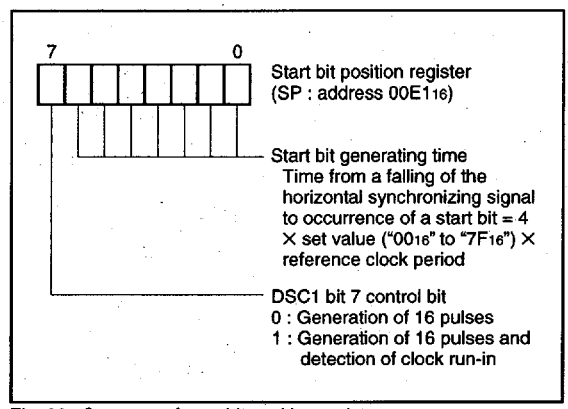


Fig. 26. Structure of start bit position register

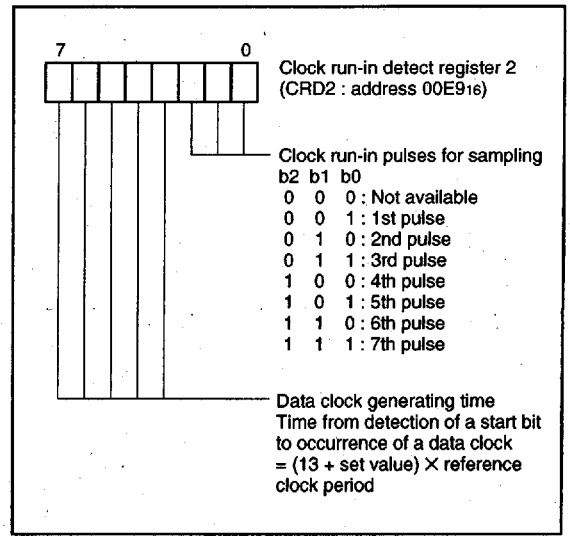


Fig. 27. Structure of clock run-in detect register 2

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
M37267EE-XXXSP, M37267EESP

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(8) Clock run-in determination circuit

This circuit sets a window in the clock run-in portion in the composite video signal, and then determinates clock run-in by counting the number of pulses in this window. Set the time from a falling of the horizontal synchronizing signal to a start of the window by bits 0 to 5 of the window register (address $00E2_{16}$; refer to Figure 28). The window ends according to the contents of the setting of the start bit position register (refer to Figure 26).

The count value of pulses in the window is stored in clock run-in register 1 (address $00E6_{16}$; refer to Figure 29). When this count value is 4 to 6, it is determined as a clock run-in. Accordingly, set the count value so that the window may start after the first pulse of the clock run-in (refer to Figure 30).

The contents to be set in the window register are written at a falling of the horizontal synchronizing signal. For this reason, even if an instruction for setting is executed, the contents of the register cannot be rewritten until a falling of the horizontal synchronizing signal.

Reference clock is counted in the period from a falling of the clock pulse set in bits 0 to 2 of the clock run-in detect register 2 (address $00E9_{16}$) to the next falling. The count value is stored in bits 3 to 7 of the clock run-in detect register 1 (address $00E8_{16}$) (When the count value exceeds "$1F_{16}$," "$1F_{16}$" is held). Read out these bits after the occurence of a data slicer interrupt (refer to (11) Interrupt Request Generating Circuit).

Figure 31 shows the structure of clock run-in detect register 1.

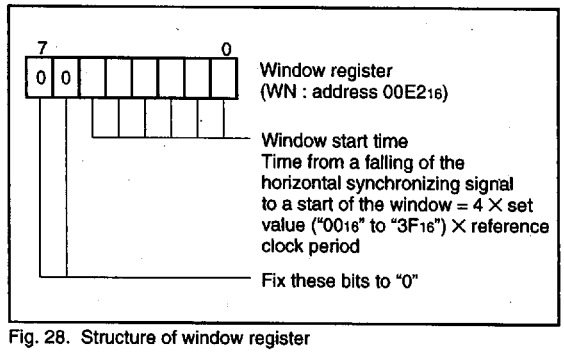

Fig. 28. Structure of window register

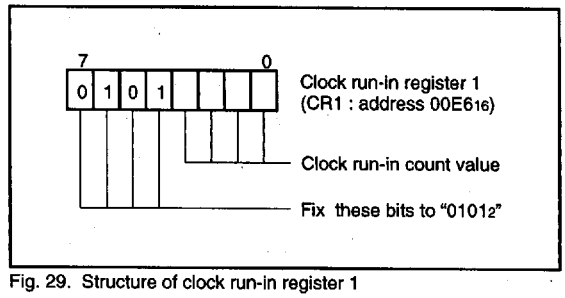

Fig. 29. Structure of clock run-in register 1

(9) Data clock generating circuit

This circuit generates a data clock phase-synchronized with the start bit detected in the start bit detecting circuit.

Set the time from detection of the start bit to occurrence of the data clock in bits 3 to 7 of the clock run-in detect register 2 (address $00E9_{16}$). The time to be set is represented by the following expression:

Time = (13 + set value) × reference clock period (at X_{IN} = 8 MHz)

For a data clock, 16 pulses are generated. When just 16 pulses have been generated, bit 7 of the data slicer control register is set to "1" (refer to Figure 19). When method 1 is already selected as a start bit detecting method, this bit becomes a logical product (AND) value with a clock run-in determination result by setting bit 7 of the start bit position register to "1."

When method 2 is already selected as a start bit detecting method and 16 pulses are generated of a data clock regardless of bit 7 of the start bit position register, this bit is set to "1." The contents of this bit are reset at a falling of the vertical synchronizing signal (V_{SEP}).

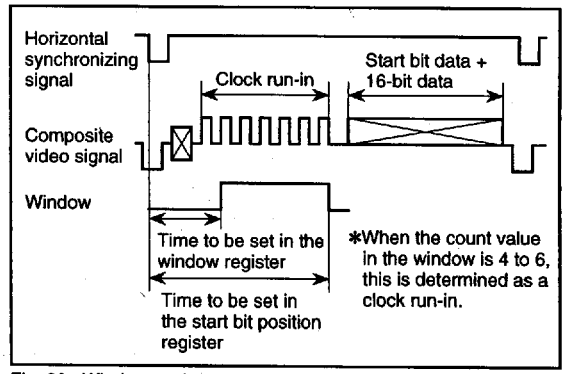

Fig. 30. Window setting

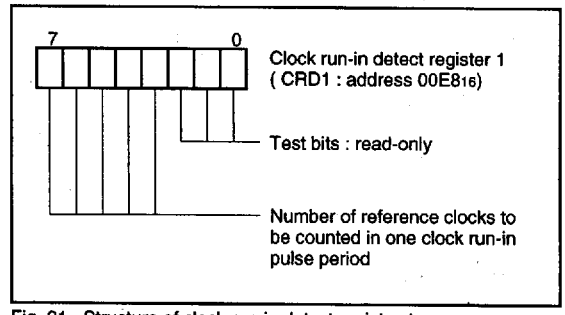

Fig. 31. Structure of clock run-in detect register 1

(10) 16-bit Shift Register

The caption data converted into a digital value by the comparator is stored into the16-bit shift register in synchronization with the data clock. The contents of the high-order 8 bits of the stored caption data and the contents of the low-order 8 bits of the same data can be obtained by reading out the data register 2 (address 00E5$_{16}$) and data register 1 (address 00E4$_{16}$), respectively. These registers are reset to "0" at a falling of V_{sep}. Read out data registers 1 and 2 after the occurence of a data slicer interrupt (refer to (11) Interrupt Request Generating Circuit).

(11) Interrupt Request Generating Circuit

A data slicer interrupt request occurs concurrently with an end of the line specified in the caption position register (address 00E0$_{16}$), a falling of the composite sync signal. Read out the contents of data registers 1 and 2 and the contents of bits 3 to 7 of the clock run-in detect register 1 after the occurence of a data slicer interrupt request.

(12) Synchronizing Signal Counter

The synchronizing signal counter counts the composite sync signal taken out from a video signal in the data slicer circuit or the vertical synchronizing signal V_{sep} as a count source.

The count value in a certain time (T time) generated by $f(X_{IN})/2^{13}$ or $f(X_{IN})/2^{21}$ is stored into the 5-bit latch. Accordingly, the latch value changes in the cycle of T time. When the count value exceeds "1F$_{16}$," "1F$_{16}$" is stored into the latch.

The latch value can be obtained by reading out the sync pulse counter register (address 00EA$_{16}$). A count source is selected by bit 5 of the sync pulse counter register. The count time (T time) varies depending on the selected count source.

When the HSYNC signal has been selected as a reference clock source in the status which bit 1 of the data slicer control register 2 (address 00DF$_{16}$) is set to "1," the synchronizing signal counter cannot be used.

Figure 32 shows the structure of the sync pulse counter and Figure 33 shows the synchronizing signal counter block diagram.

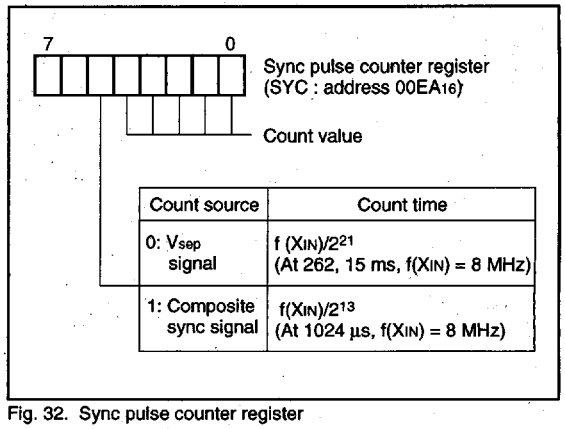

Fig. 32. Sync pulse counter register

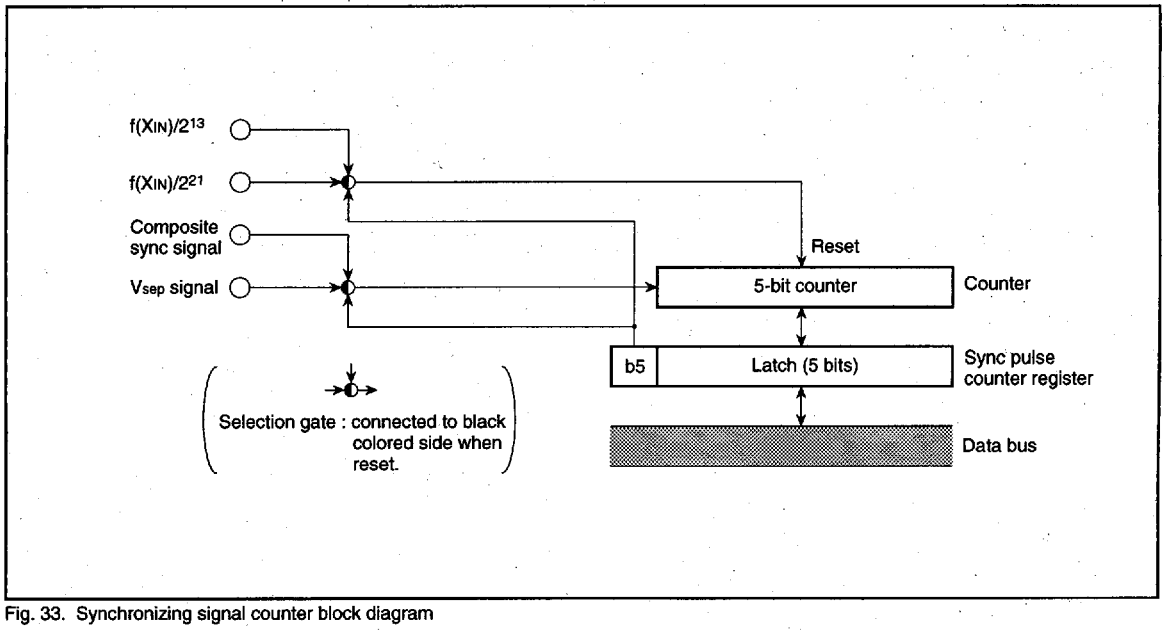

Fig. 33. Synchronizing signal counter block diagram

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
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MULTI-MASTER I²C-BUS INTERFACE

The multi-master I²C-BUS interface is a circuit for serial communications conformed with the Philips I²C-BUS data transfer format. This interface, having an arbitration lost detection function and a synchronous function, is useful for serial communications of the multi-master.

Figure 34 shows a block diagram of the multi-master I²C-BUS interface and Table 3 shows multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C address register, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register and other control circuits.

Table 3. Multi-master I²C-BUS interface functions

Item	Function
Format	In conformity with Philips I²C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I²C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ = 4 MHz)

ϕ : System clock = f(XIN)/2

Note: We are not responsible for any third party's infringement of patent rights or other rights attributable to the use of the control function (bits 6 and 7 of the I²C control register at address 00F9₁₆) for connections between the I²C-BUS interface and ports (SCL1, SCL2, SDA1, SDA2).

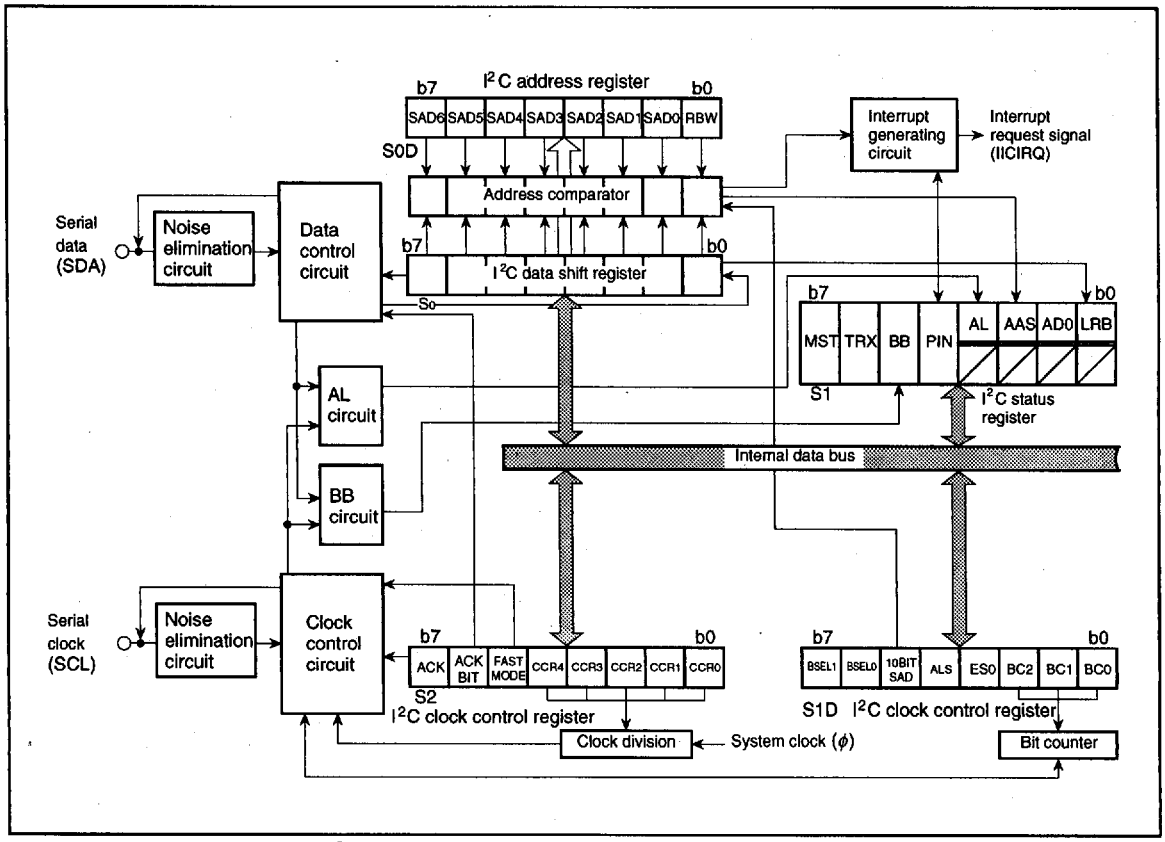


Fig. 34. Block diagram of multi-master I²C-BUS interface

(1) I²C Data Shift Register

The I²C data shift register (S0 : address 00F6₁₆) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted one bit to the left.

The I²C data shift register is in a write enable status only when the ES0 bit of the I²C control register (address 00F9₁₆) is "1." The bit counter is reset by a write instruction to the I²C data shift register. When both the ES0 bit and the MST bit of the I²C status register (address 00F8₁₆) are "1," the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ES0 bit value.

Note: To write data into the I²C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

(2) I²C Address Register

The I²C address register (address 00F7₁₆) consists of a 7-bit slave address and a read/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition are detected.

■ Bit 0: Read/write bit (RBW)

Not used in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RBW) of the I²C address register.

The RBW bit is cleared to "0" automatically when the stop condition is detected.

■ Bits 1 to 7: Slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

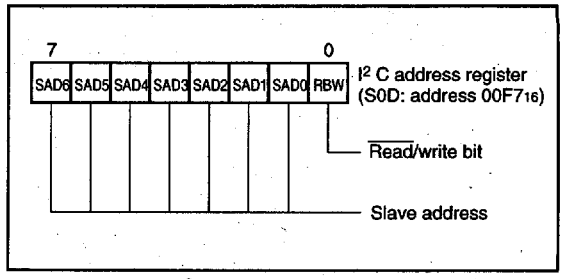


Fig. 35. Structure of I²C address register

(3) I²C Clock Control Register

The I²C clock control register (address 00FA₁₆) is used to set ACK control, SCL mode and SCL frequency.

■ Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 4.

■ Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0," the standard clock mode is set. When the bit is set to "1," the high-speed clock mode is set.

■ Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0," the ACK return mode is set and make SDA "L" at the occurrence of an ACK clock. When the bit is set to "1," the ACK non-return mode is set. The SDA is held in the "H" status at the occurrence of an ACK clock.

However, when the slave address matches the address data in the reception of address data at ACK BIT = "0," the SDA is automatically made "L" (ACK is returned). If there is a mismatch between the slave address and the address data, the SDA is automatically made "H"(ACK is not returned).

*ACK clock: Clock for acknowledgement

■ Bit 7: ACK clock bit (ACK)

This bit specifies a mode of acknowledgment which is an acknowledgment response of data transmission. When this bit is set to "0," the no ACK clock mode is set. In this case, no ACK clock occurs after data transmission. When the bit is set to "1," the ACK clock mode is set and the master generates an ACK clock upon completion of each 1-byte data transmission.The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (make SDA "H") and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transmitting. If data is written during transmitting, the I²C clock generator is reset, so that data cannot be transmitted normally.

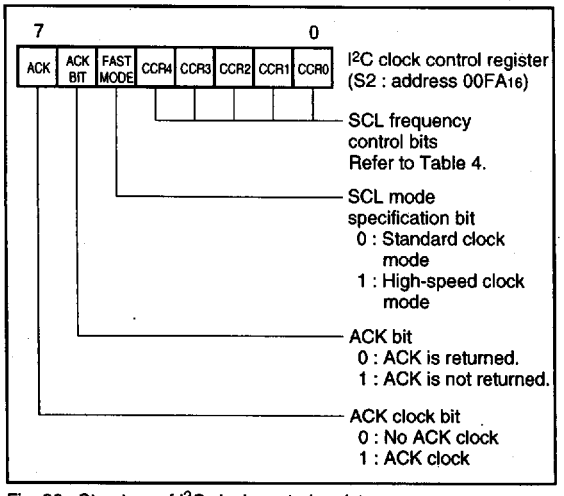


Fig. 36. Structure of I²C clock control register

Table 4. Set values of I²C clock control register and SCL frequency

Setting value of CCR4–CCR0					SCL frequency (at ϕ = 4MHz, unit : kHz)	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard clock mode	High-speed clock mode
0	0	0	0	0	Setting disabled	Setting disabled
0	0	0	0	1	Setting disabled	Setting disabled
0	0	0	1	0	Setting disabled	Setting disabled
0	0	0	1	1	Setting disabled	333
0	0	1	0	0	Setting disabled	250
0	0	1	0	1	100	400(Note)
0	0	1	1	0	83.3	166
⋮	⋮	⋮	⋮	⋮	500/CCR value	1000/CCR value
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Note: At 400 kHz in the high-speed clock mode, the duty is 40%. In the other cases, the duty is 50%.

(4) I²C Control Register

The I²C control register (address 00F916) controls data communication format.

■ Bits 0 to 2: Bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. An interrupt request signal occurs immediately after the number of bits specified with these bits are transmitted.

When a START condition is received, these bits become "0002" and the address data is always transmitted and received in 8 bits.

■ Bit 3: I²C interface use enable bit (ES0)

This bit enables to use the multimaster I²C BUS interface. When this bit is set to "0," the use disable status is provided, so the SDA and the SCL become high-impedance. When the bit is set to "1," use of the interface is enabled.

When ES0 = "0," the following is performed.

- PIN = "1," BB = "0" and AL = "0" are set (they are bits of the I²C status register at address 00F816).
- Writing data to the I²C data shift register (address 00F616) is disabled.

■ Bit 4: Data format selection bit (ALS)

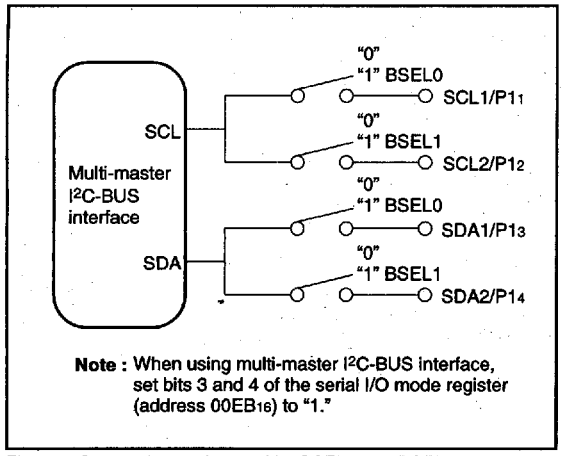
This bit decides whether or not to recognize slave addresses. When this bit is set to "0," the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "(5) I²C Status Register," bit 1) is received, transmission processing can be performed. When this bit is set to "1," the free data format is selected, so that slave addresses are not recognized.

■ Bit 5: Addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0," the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (address 00F716) are compared with address data. When this bit is set to "1," the 10-bit addressing format is selected, all the bits of the I²C address register are compared with address data.

■ Bits 6 and 7: Connection control bits between I²C-BUS interface and ports (BSEL0, BSEL1)

These bits controls the connection between SCL and ports or SDA and ports (refer to Figure 37).



Note : When using multi-master I²C-BUS interface, set bits 3 and 4 of the serial I/O mode register (address 00EB16) to "1."

Fig. 37. Connection port control by BSEL0 and BSEL1

(5) I²C Status Register

The I²C status register (address 00F816) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

■ Bit 0: Last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00F616).

■ Bit 1: General call detecting flag (AD0)

This bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition.

*General call: The master transmits the general call address "0016" to all slaves.

■ Bit 2: Slave address comparison flag (AAS)

This flag indicates a comparison result of address data.

①In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions.
- The address data immediately after occurrence of a START condition agrees with the slave address stored in the high-order 7 bits of the I²C address register (address 00F716).
- A general call is received.

②In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition.
- When the address data is compared with the I²C address register (8 bits consisted of slave address and RBW), the first bytes agree.

③ The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00F616).

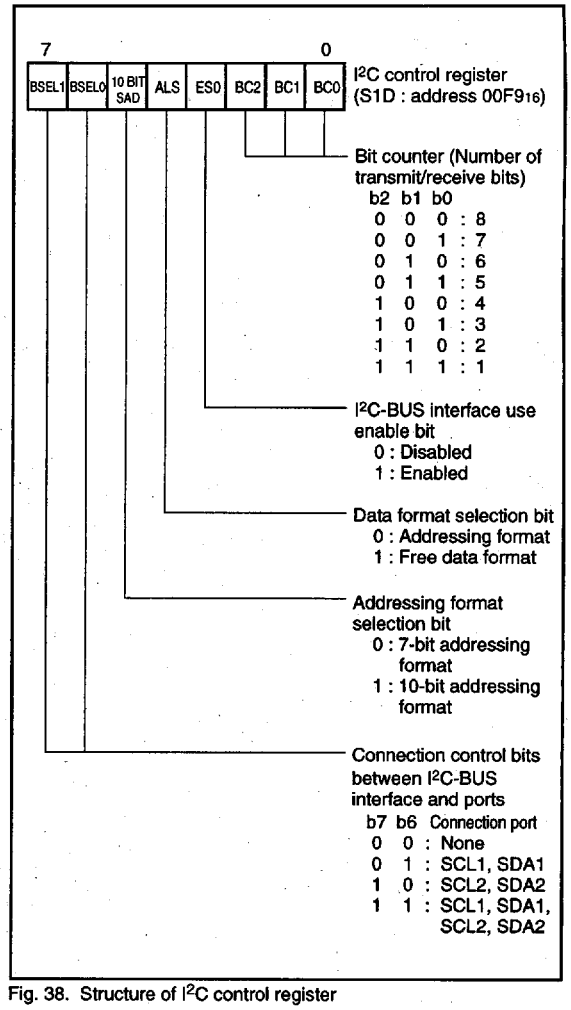


Fig. 38. Structure of I²C control register

■ Bit 3: Arbitration lost* detecting flag (AL)

In the master transmission mode, when the SDA is made "L" by any other device, arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." In the case arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to receive and recognize its own slave address transmitted by another master device.

*Arbitration lost: The status in which communication as a master is disabled.

■ Bit 4: I^2C-BUS interface interrupt request bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the state of the PIN bit changes from "1" to "0." At the same time, an interrupt request signal occurs to the CPU. The PIN bit is set to "0" in synchronization with a falling of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling of the PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 40 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in one of the following conditions.

- Executing a write instruction to the I^2C data shift register (address $00F6_{16}$).
- When the ES0 bit is "0"
- At reset

The conditions in which the PIN bit is set to "0" are shown below:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

■ Bit 5: Bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. When this bit is set to "1," this bus system is busy and the occurrence of a START condition is disabled by the START condition duplication prevention function (Note).

This flag can be written by software only in the master transmission mode. In the other modes, this bit is set to "1" by detecting a START condition and set to "0" by detecting a STOP condition. When the ES0 bit of the I^2C control register (address $00F9_{16}$) is "0" and at reset, the BB flag is kept in the "0" state.

■ Bit 6: Communication mode specification bit (transfer direction specification bit: TRX)

This bit decides a direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output onto the SDA in synchronization with the clock generated on the SCL.

When the ALS bit of the I^2C control register (address $00F9_{16}$) is "0" in the slave reception mode is selected, the TRX bit is set to "1" (transmit) if the least significant bit ($R/\overline{W}$ bit) of the address data transmitted by the master is "1." When the ALS bit is "0" and the $R/\overline{W}$ bit is "0," the TRX bit is cleared to "0" (receive).

The TRX bit is cleared to "0" in one of the following conditions.

- When arbitration lost is detected.
- When a STOP condition is detected.
- When occurence of a START condition is disabled by the START condition duplication preventing function (Note).
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

■ Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is "0," the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1," the master is specified and a START condition and a STOP condition are generated, and also the clocks required for data communication are generated on the SCL.

The MST bit is cleared to "0" in one of the following conditions.

- Immediately after completion of 1-byte data transmission when arbitration lost is detected
- When a STOP condition is detected.
- When occurence of a START condition is disabled by the START condition duplication preventing function (Note).
- At reset

Note: The START condition duplication prevention function disables the occurence of a START condition, reset of bit counter and SCL output when the following condition is satisfied:
• a START condition is set by another master device.

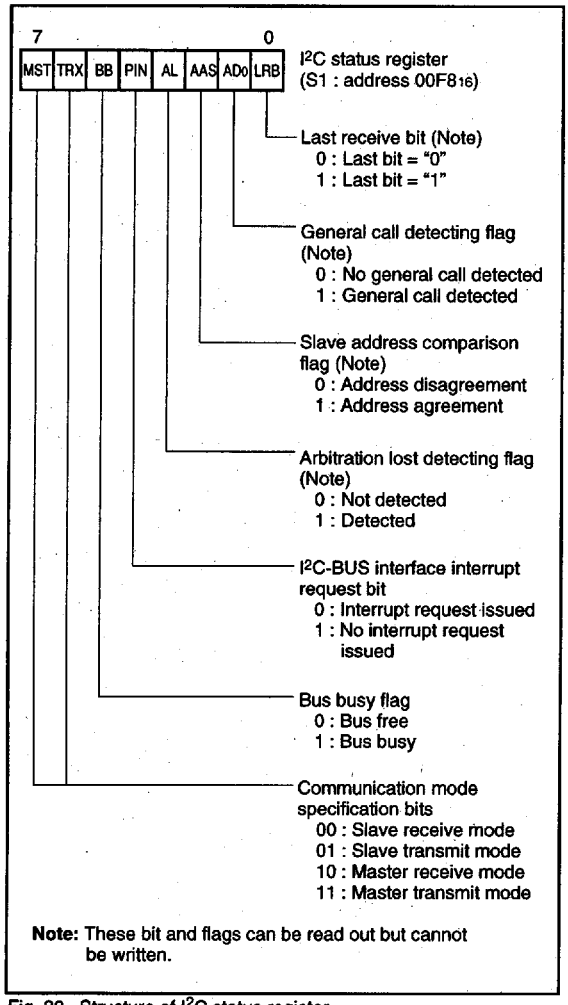


Fig. 39. Structure of I²C status register

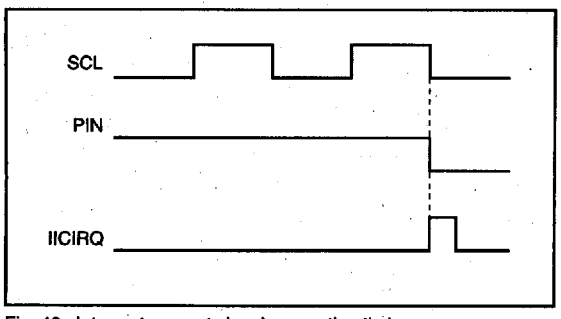


Fig. 40. Interrupt request signal generating timing

(6) START Condition Generating Method

When the ES0 bit of the I²C control register (address 00F916) is "1," execute a write instruction to the I²C status register (address 00F816) for setting the MST, TRX and BB bits to "1." Then a START condition occurs. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generating timing and BB bit set timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 41, the START condition generating timing diagram, and Table 5, the START condition/STOP condition generating timing table.

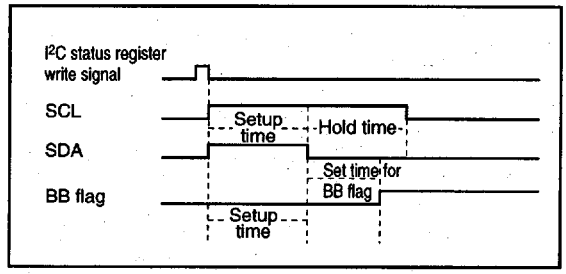


Fig. 41. START condition generating timing diagram

(7) STOP Condition Generating Method

When the ES0 bit of the I²C control register (address 00F916) is "1," execute a write instruction to the I²C status register (address 00F816) for setting the MST bit and the TRX bit to "1" and the BB bit to "0". Then a STOP condition occurs. The STOP condition generating timing and the BB flag reset timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 42, the STOP condition generating timing diagram, and Table 5, the START condition/STOP condition generating timing table.

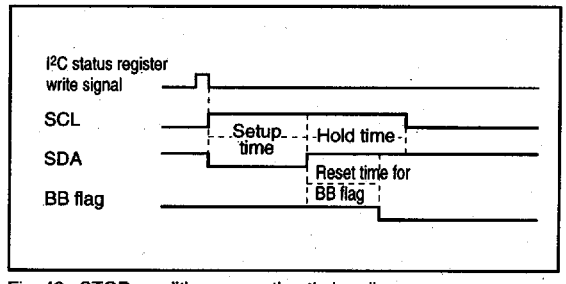


Fig. 42. STOP condition generating timing diagram

Table 5. START condition/STOP condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 μs (20 cycles)	2.5 μs (10 cycles)
Hold time	5.0 μs (20 cycles)	2.5 μs (10 cycles)
Set/reset time for BB flag	3.0 μs (12 cycles)	1.5 μs (6 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

(8) START/STOP Condition Detecting Conditions

The START/STOP condition detecting conditions are shown in Figure 43 and Table 6. Only when the 3 conditions of Table 5 are satisfied, a START/STOP condition can be detected.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" occurs to the CPU.

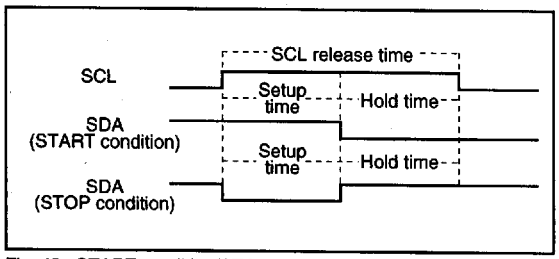


Fig. 43. START condition/STOP condition detecting timing diagram

Table 6. START condition/STOP condition detecting conditions

Standard clock mode	High-speed clock mode
6.5 μs (26 cycles) < SCL release time	1.0 μs (4 cycles) < SCL release time
3.25 μs (13 cycles) < Setup time	0.5 μs (2 cycles) < Setup time
3.25 μs (13 cycles) < Hold time	0.5 μs (2 cycles) < Hold time

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

(9) Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats is described below.

①7-bit addressing format

To meet the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 00F9₁₆) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C address register (address 00F7₁₆). At the time of this comparison, address comparison of the RBW bit of the I²C address register (address 00F7₁₆) is not made. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 44, (1) and (2).

②10-bit addressing format

To meet the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (address 00F9₁₆) to "1." An address comparison is made between the first-byte address data transmitted from the master and the 7-bit slave address stored in the I²C address register (address 00F7₁₆). At the time of this comparison, an address comparison between the RBW bit of the I²C address register (address 00F7₁₆) and the R/$\overline{W}$ bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the R/$\overline{W}$ bit which is the last bit of the address data not only specifies the direction of communication for control data but also is processed as an address data bit.

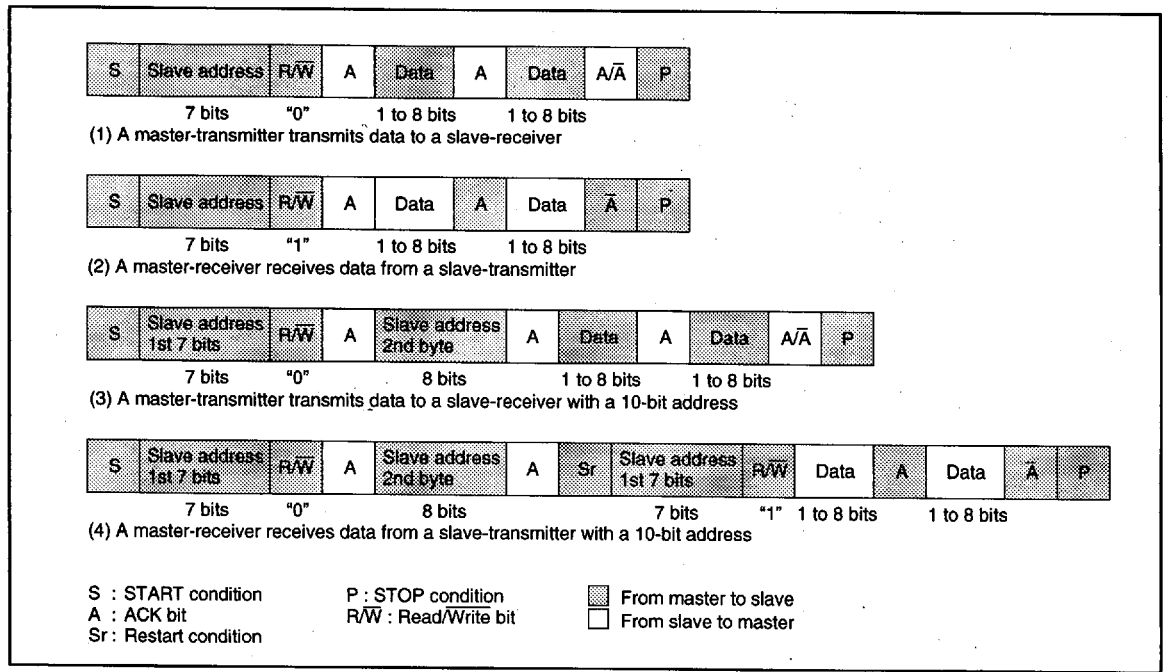


Fig. 44. Address data communication format

When the first-byte address data matches the slave address, the AAS bit of the I²C status register (address 00F8₁₆) is set to "1." After the second-byte address data is stored into the I²C data shift register (address 00F6₁₆), make an address comparison between the second-byte data and the slave address by software. When the address data of the 2 bytes matches the slave address, set the RBW bit of the I²C address register (address 00F7₁₆) to "1" by software. This processing can match the 7-bit slave address and R/$\overline{W}$ data, which are received after a RESTART condition is detected, with the value of the I²C address register (address 00F7₁₆). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 44, (3) and (4).

(10) Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

① Set a slave address in the high-order 7 bits of the I²C address register (address 00F7₁₆) and "0" in the RBW bit.
② Set the ACK return mode and SCL = 100 kHz by setting "85₁₆" in the I²C clock control register (address 00FA₁₆).
③ Set "10₁₆" in the I²C status register (address 00F8₁₆) and hold the SCL at the "H" level.
④ Set a communication enable status by setting "48₁₆" in the I²C control register (address 00F9₁₆).
⑤ Set the address data of the destination of transmission in the high-order 7 bits of the I²C data shift register (address 00F6₁₆) and set "0" in the least significant bit.
⑥ Set "F0₁₆" in the I²C status register (address 00F8₁₆) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occurs.
⑦ Set transmit data in the I²C data shift register (address 00F6₁₆). At this time, an SCL and an ACK clock automatically occurs.
⑧ When transmitting control data of more than 1 byte, repeat step ⑦.
⑨ Set "D0₁₆" in the I²C status register (address 00F8₁₆). After this, if ACK is not returned or transmission ends, a STOP condition occurs.

(11) Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode and using the addressing format is shown below.

① Set a slave address in the high-order 7 bits of the I²C address register (address 00F7₁₆) and "0" in the RBW bit.
② Set the no ACK clock mode and SCL = 400 kHz by setting "25₁₆" in the I²C clock control register (address 00FA₁₆).
③ Set "10₁₆" in the I²C status register (address 00F8₁₆) and hold the SCL at the "H" level.
④ Set a communication enable status by setting "48₁₆" in the I²C control register (address 00F9₁₆).
⑤ When a START condition is received, an address comparison is made.
⑥ •When all transmitted addresses are "0" (general call)
AD0 of the I²C status register (address 00F8₁₆) is set to "1" and an interrupt request signal occurs.
•When the transmitted addresses match the address set in ①
ASS of the I²C status register (address 00F8₁₆) is set to "1" and an interrupt request signal occurs.
•In the cases other than the above
AD0 and AAS of the I²C status register (address 00F8₁₆) are set to "0" and no interrupt request signal occurs.
⑦ Set dummy data in the I²C data shift register (address 00F6₁₆).
⑧ When receiving control data of more than 1 byte, repeat step ⑦.
⑨ When a STOP condition is detected, the communication ends.

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
M37267EE-XXXSP, M37267EESP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 7 outlines the CRT display functions of the M37267M6-XXXSP.

The M37267M6-XXXSP incorporates a CRT display control circuit of 34 characters × 4 lines. CRT display is controlled by the CRT control register. Up to 192 kinds of characters can be displayed. The colors can be specified for each character. A combination of up to 7 colors can be obtained by using each output signal (R, G, and B).

The character area for one character is 8 × 13 dots. However, as a 2-dot blank and an 1-dot underline area are provided in the vertical direction, the display character consist of 8 × 10 dots. When 1 dot is used as a space with an adjacent character in the horizontal direction, the display character has a structure of 7 × 10 dots. There is also a rounding function of 6 × 9 dots shifted by 1/2 inside the said structure of 7 × 10 dots, so this function permits display of a smooth character pattern (refer to Figure 45).

The following shows the procedure how to display characters on the CRT screen.

① Specify the display mode by using the display mode register.
② Write the display character code and attribute code to the RAM for display.
③ Specify the vertical position by using the vertical position register.
④ Specify the character size by using the character size register.
⑤ Specify the horizontal position by using the horizontal position register.
⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT display starts according to the input of the VSYNC signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (4 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

The M37267M6-XXXSP includes the mixing circuit that can be output the signal mixed external color signals with internal color signals, so that the CRT display can be controlled by the 2-chip constructed system.

The display in the area subsequent to an arbitrary scanning line can be concealed by masking the display screen area. Using this function and decrementing the vertical position register in each vertical synchronization period by software can smoothly roll-up (Smooth Roll-up) the display screen.

Figure 46 shows the block diagram of the CRT display control circuit.
Figure 47 shows the structure of the CRT display control register.
Figure 48 shows the structure of the display mode register.

Table 7. Outline of CRT display functions

Parameter		Functions
Number of display characters		34 characters × 4 lines (maximum 16 lines)
Dot structure		CCD mode : 8 × 13 dots OSD mode : 8 × 10 dots (Character : 8 × 10 dots in both modes)
Kinds of characters		256 kinds
Kinds of character sizes		5 kinds
Color	Kinds of colors	maximum 7 kinds
	Coloring unit	A character
Display expansion		Possible (multiline display)
Attribute		Italic, underline, flash
Text display		15 lines
Raster coloring		Possible (maximum 7 kinds)
Smooth Roll-up		Possible
Character background coloring		Possible (a screen unit, maximum 7 kinds) Switching to character color is possible
Mixing		Mixing of external and internal R, G, B, OUT1 signal is possible

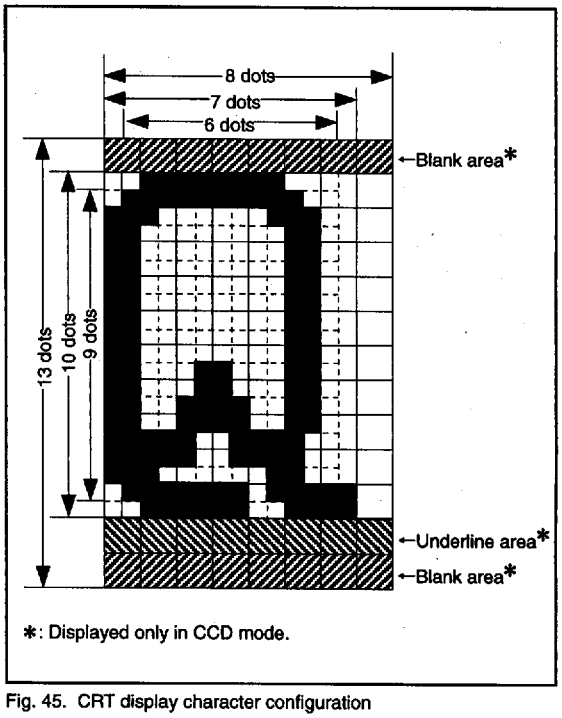


Fig. 45. CRT display character configuration

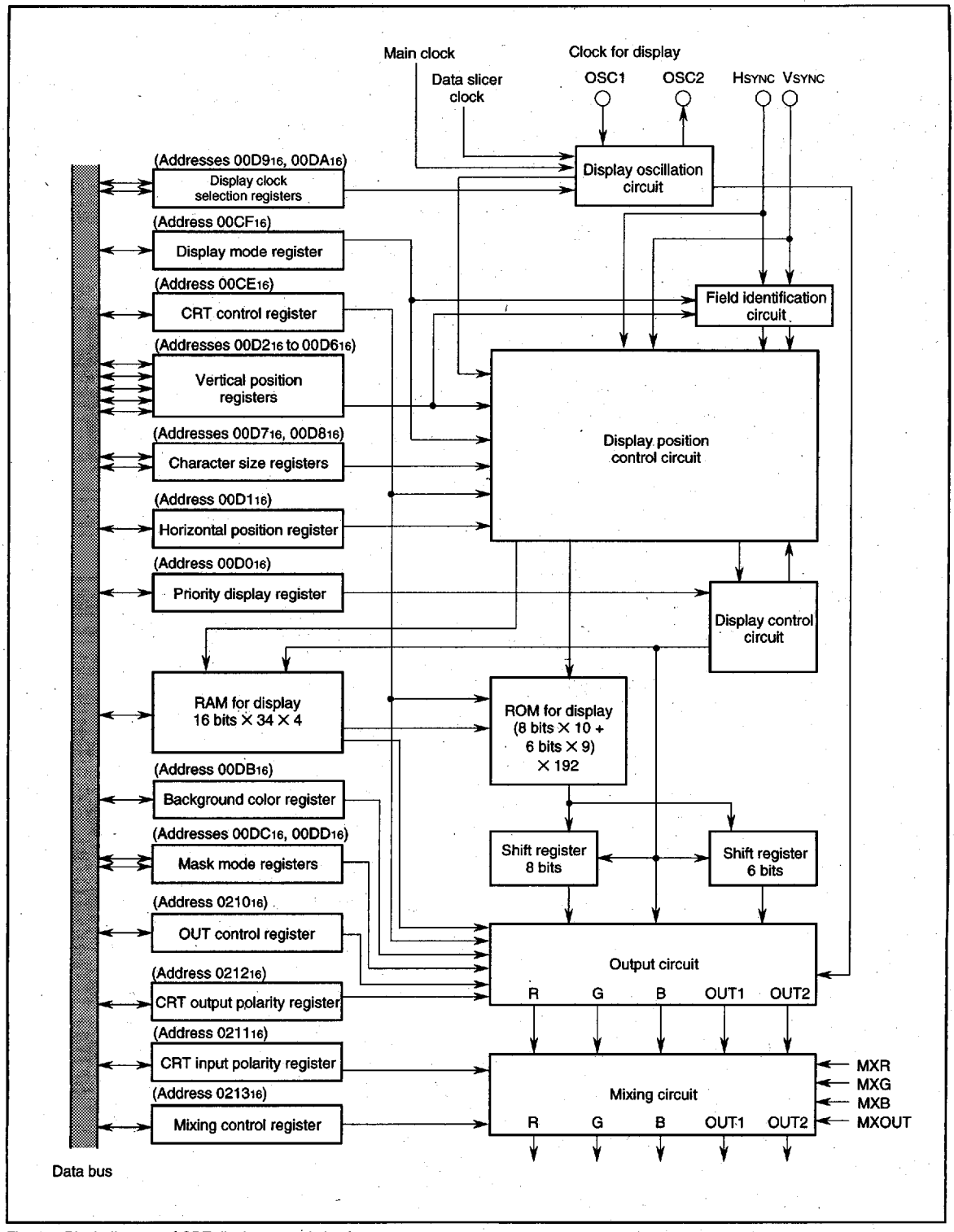


Fig. 46. Block diagram of CRT display control circuit

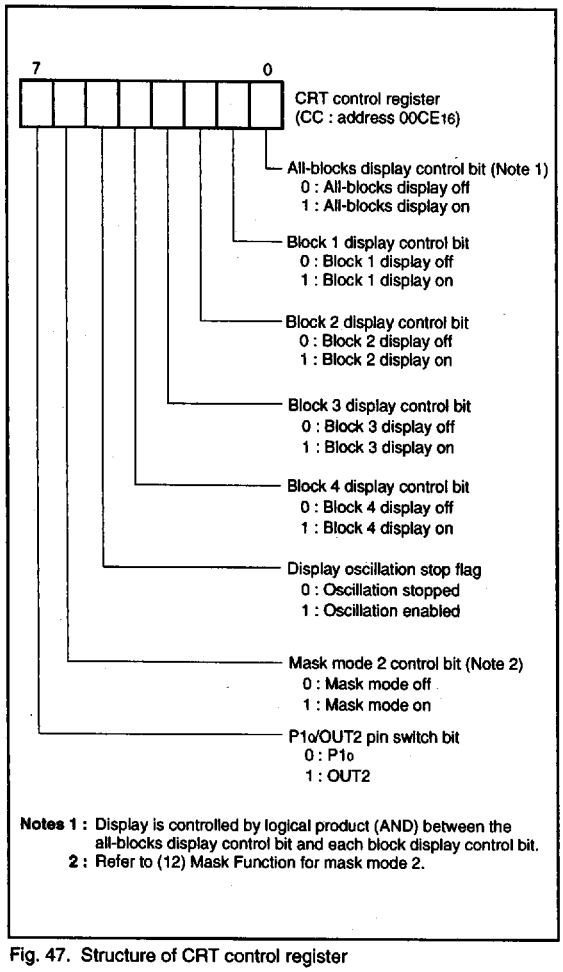


Fig. 47. Structure of CRT control register

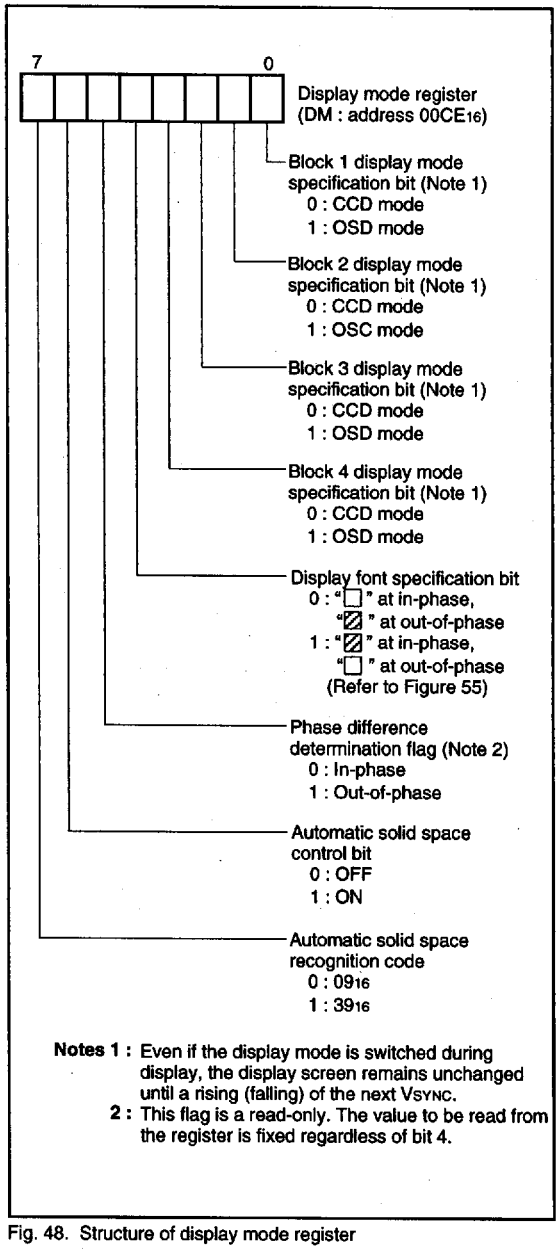


Fig. 48. Structure of display mode register

(2) Display Position

The display positions of characters are specified in units called a "block." There are 4 blocks, blocks 1 to 4. Up to 34 characters can be displayed in each block (refer to (6) Memory for Display).

The display position of each block can be set in both horizontal and vertical directions by software.

The display position in the horizontal direction can be selected for all blocks in common from 128-step display positions in units of 4Tc (Tc = oscillating cycle for display).

The display position in the vertical direction for each block can be selected from 512-step display positions in units of single scanning line.

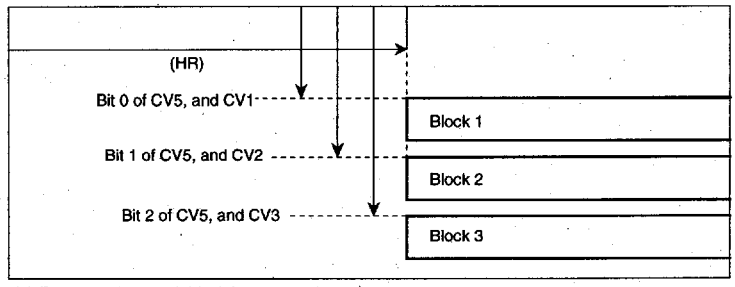
Blocks are displayed in conformance with the following rules:

① When the display position is overlapped with another block (Figure 49, (b)), a lower block number (1 to 4) is displayed on the front.

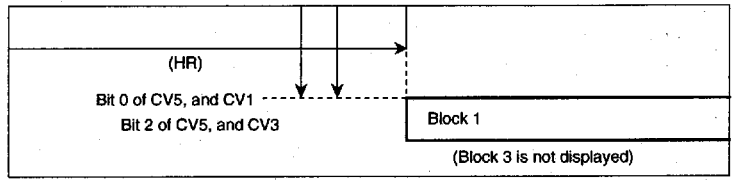
② When another block display position appears while one block is displayed, the block with a larger set value as the vertical display start position is displayed.

③ In the case of a block (block 1 or 2) for which "priority display" is already set by the priority display control register, this block is displayed with top priority regardless of ① and ② above (Figure 49, (d)).

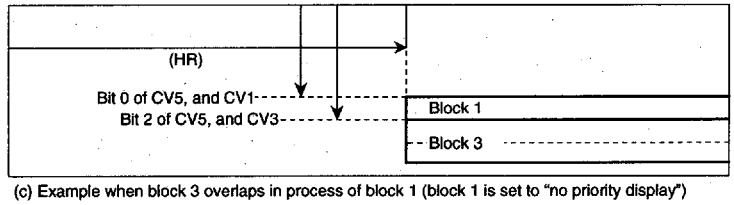
④ In the case both blocks are of "priority display", they are displayed in conformance with rule of ②. For the priority display function, refer to (13) Priority Function.



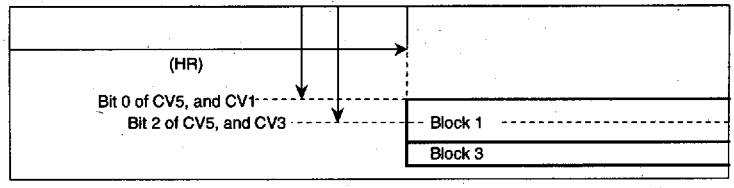
(a) Example when each block is separated



(b) Example when block 3 overlaps with block 1



(c) Example when block 3 overlaps in process of block 1 (block 1 is set to "no priority display")



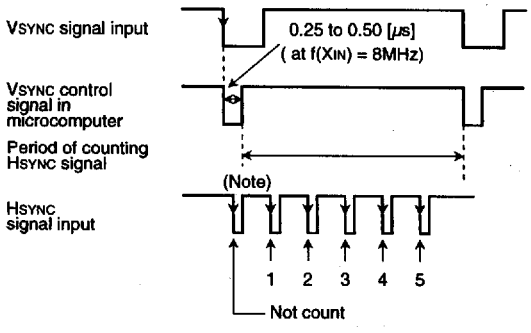
(d) Example when block 3 overlaps in process of block 1 (block 1 is set to "priority display")

Note : CVX (X : 1 to 5) indicates the contents of vertical position registers.

Fig. 49. Display position

The display position in the vertical direction is determined by counting the horizontal sync signal (HSYNC). At this time, it starts to count the rising edge (falling edge) of HSYNC signal from after about 1 machine cycle of rising edge (falling edge) of VSYNC signal. So interval from rising edge (falling edge) of VSYNC signal to rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of HSYNC and VSYNC signals can select with the CRT input polarity register (address 021_{16}). For details, refer to (12) CRT Output Pin Control.

Note: When bits 0 and 1 of the CRT input polarity register (address 021_{16}) are set to "1" (negative polarity), the vertical position is determined by counting falling edge of HSYNC signal after rising edge of VSYNC control signal in the microcomputer (refer to Figure 50).

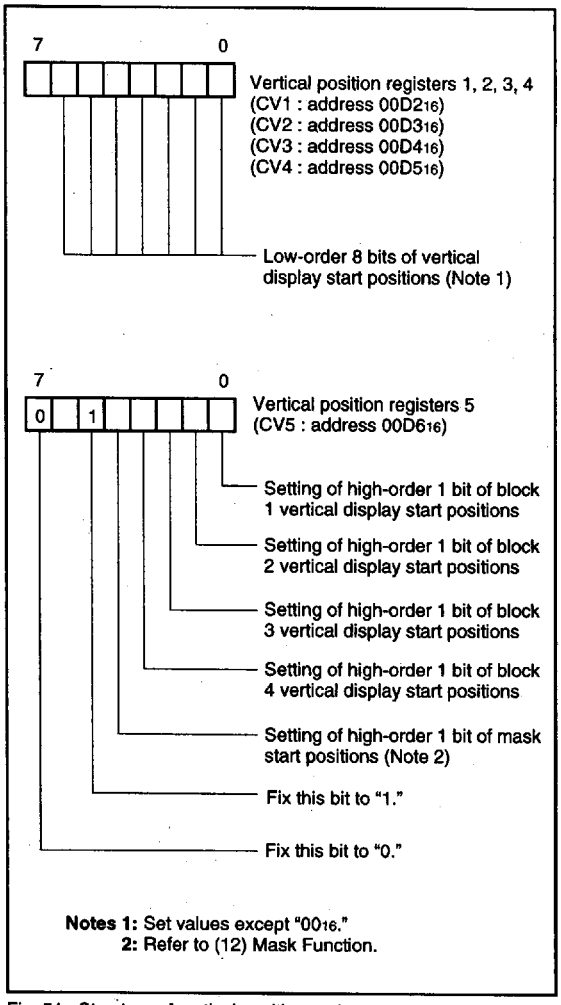


When bits 0 and 1 of the CRT input polarity register (address 021_{16}) are set to "1" (negative polarity)

Note: Do not generate falling edge of HSYNC signal near rising edge of VSYNC control signal in microcomputer to avoid jitter.

Fig. 50. Supplement explanation for display position

The vertical position for each block can be set in 512 steps (where each step is one scanning line) as values "01_{16}" to "$7F_{16}$" in vertical position registers 1 to 4 (addresses $00D2_{16}$ to $00D5_{16}$) and values "0_{16}" to "F_{16}" in bits 0 to 3 of the vertical position register 5 (address $00D6_{16}$). The structure of the vertical position register is shown in Figure 51.



Notes 1: Set values except "00_{16}."
2: Refer to (12) Mask Function.

Fig. 51. Structure of vertical position registers

The horizontal position is common to all blocks, and can be set in 128 steps (where 1 step is 4Tc, Tc being the display oscillation period) as values "00_{16}" to "$7F_{16}$" in bits 0 to 5 of the horizontal position register (address $00D1_{16}$). The structure of the horizontal position register is shown in Figure 52.

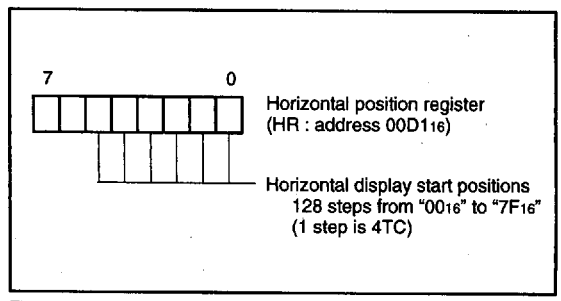


Fig. 52. Structure of horizontal position register

(3) Character Size

The size of characters to be displayed can be from 5 sizes for each block. Use the character size register (addresses 00D716 and 00D816) to set a character size. The character size of block 1 can be specified by using bits 2 to 0 of the character size register; the character size of block 2 can be specified by using bits 6 to 4; the character size of block 3 can be specified by using bits 2 to 0 in the character size register 2; the character size of block 4 can be specified by using bits 6 to 4. Figure 53 shows the structure of the character size register. The character size can be selected from 3 sizes: minimum size, medium size and large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the oscillating cycle for display (Tc) in the width (horizontal) direction. The minimum size consists of [1 scanning line] × [2Tc]; the medium size consists of [2 scanning lines] × [4Tc]; and the large size consists of [4 scanning lines] × [8Tc]. The medium and large 1/2 times size in the horizontal direction can be selected by setting bit 2 of each character size register to "1." When 1 scanning line is selected as the vertical size (minimum size), the phase difference determination display* is performed. Table 8 shows the relation between the set values in the character size register and the character sizes.

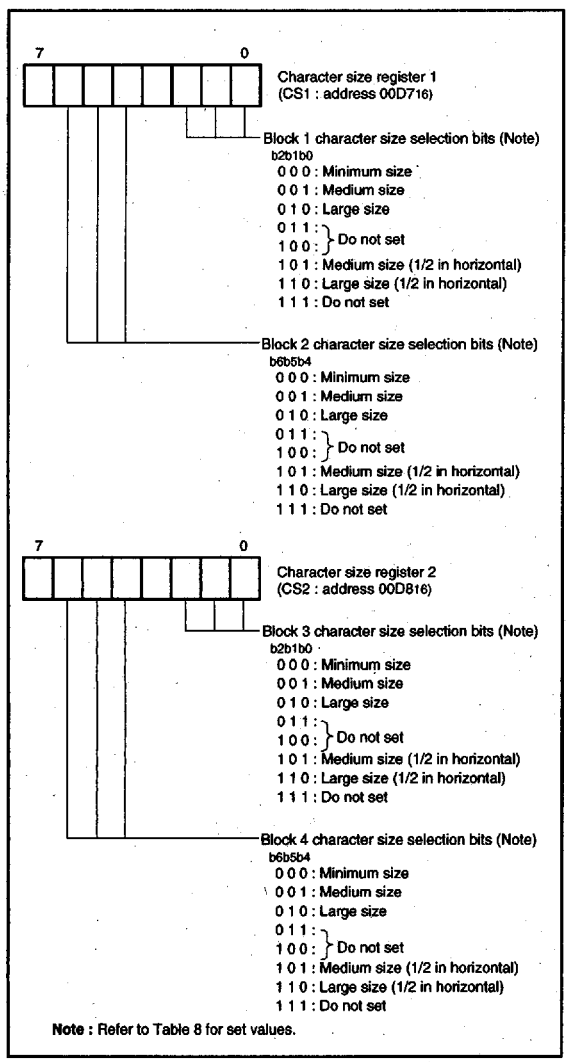


Fig. 53. Structure of character size register

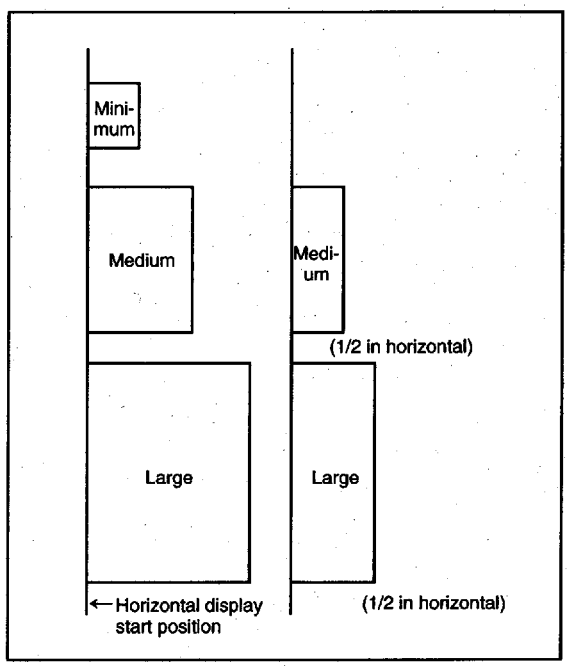


Fig. 54. Display start position of each character size (horizontal direction)

Table 8. Relation between set values in character size register and character sizes

Set values of character size register			Character size	Width (horizontal) direction Tc: oscillating cycle for display	Height (vertical) direction scanning lines
CSn_2	CSn_1	CSn_0			
0	0	0	Minimum (phase difference determination display)	2Tc	1
0	0	1	Medium	4Tc	2
0	1	0	Large	8Tc	4
0	1	1	This is not available		
1	0	0	This is not available		
1	0	1	Medium (1/2 in horizontal)	2Tc	2
1	1	0	Large (1/2 in horizontal)	4Tc	4
1	1	1	This is not available		

Notes 1: The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal display start position is common to all blocks even when the character size varies with each block (refer to Figure 54).

2: Even if the value of the character size register is rewritten during display, the display screen remains unchanged until a rising (falling) of the next V_{SYNC}.

(4) Phase difference determination display

The phase difference determination function determines whether a synchronizing signal of interlacing system is in an in-phase field or an out-of-phase field through differences in their waveform, and displays a 1-character font in both fields.

In the following, the phase difference determination standard for the case where both the horizontal sync signal and the vertical sync signal are negative-polarity inputs will be explained. A phase difference is determined by detecting the time from a falling edge of the horizontal sync signal untill a falling edge of the V_{SYNC} control signal (refer to Figure 50.) in the microcomputer and then comparing this time with the time of the previous field. When the time is longer than the comparing time, it is regarded as out-of-phase. When the time is shorter, it is regarded as in-phase. A 1-character font can be displayed in both fields by displaying 1 dot in the out-of-phase field and displaying 1 dot in the in-phase field.

The phase difference determination flag changes when a rising edge of the V_{SYNC} control signal in the microcomputer is detected.

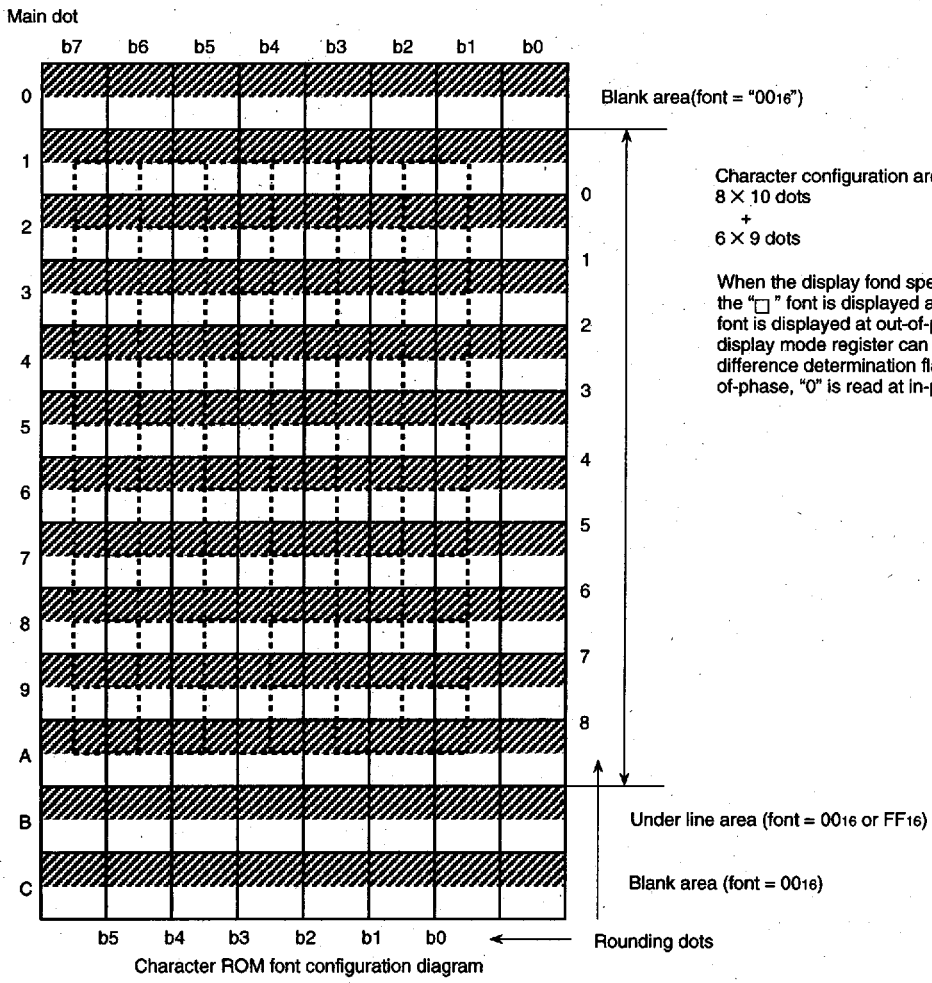
The contents of this field can be read out by the phase difference determination flag (bit 5 of the display mode register at address $00CF_{16}$). A display font is specified by bit 4 of the display mode register to select a phase with which the split font is to be displayed (refer to Figure 55).

However, the phase difference determination flag read out from the CPU is fixed to "0" at in-phase or "1" at out-of-phase, regardless of the value of the display font specification bit.

Both HSYNC signal and VSYNC signal are negative-polarity input

HSYNC		Phase	Phase difference determination flag (Note)	Display font specification bit	Display font
VSYNC control signal in microcomputer	(n-1) field (Odd-numbered) T1				
	(n) field (Even-numbered) T2	Out-of-phase	1 (T2 > T1)	0	▨ part
				1	□ part
	(n+1) field (Odd-numbered) T3	In-phase	0 (T1 < T2)	0	□ part
				1	▨ part

When using the phase difference determination flag, be sure to set bit 0 of the PWM mode register1 (address 020A16) to "0."



Character ROM font configuration diagram

Note: The phase difference determination flag changes at a rising edge of the VSYNC control signal (negative-polarity input) in the microcomputer.

Fig. 55. Relation between phrase difference determination flag and display font

(5) Clock for Display

As a clock for display to be used for CRT display, it is possible to select one of the following 3 types.

- Clock output from the data slicer
- Main clock supplied from the XIN pin
- Clock from the LC oscillator supplied from the pins OSC1 and OSC2.

This clock for display can be selected for each block by the display clock selection register (addresses 00D9$_{16}$, 00DA$_{16}$). A variety of character sizes can be obtained by combining character sizes with clocks for display. When selecting the clock from the LC oscillator as a clock for display, set bits 7 and 6 of the mixing control register (address 021316) to "1" and "0," respectively.

When selecting the main clock, set the oscillation frequency to 8 MHz.

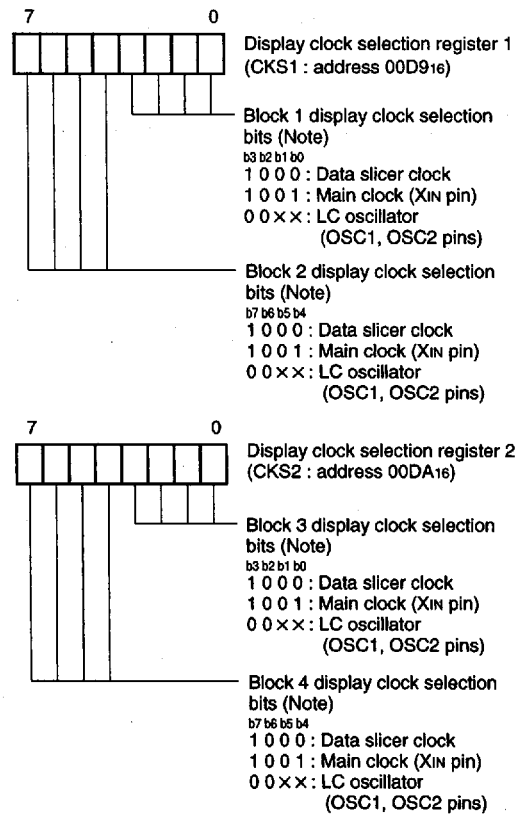


Fig. 56. Structure of display clock selection register

(6) Memory for Display

There are 2 types of memory for display : CRT display ROM (addresses 1000_{16} to $122FF_{16}$) used to store character dot data (masked) and CRT display RAM (addresses $0E00_{16}$ to $0FE1_{16}$) used to specify the colors and characters to be displayed. The following describes each type of display memory.

① ROM for display (addresses 1000_{16} to $122FF_{16}$)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM. The character code list is shown in Table 9.

The CRT display ROM has a capacity of 3648 bytes. Since 19 bytes are required for 1 character data, the ROM can stores up to 192 kinds of characters.

Within the CRT display ROM area, data for main dot font of each character that is [vertical 8 dots] × [horizontal 8 dots] is stored at addresses $1000X_{16}$ to $10BFX_{16}$ (where X = 0, 2, 4, 6, 8, A, C, E), data for rounding of each character that is [vertical 8 dots] × [horizontal 8 dots] is stored at $1000Y_{16}$ to $10BFY_{16}$ (where Y = 1, 3, 5, 7, 9, B, D, F), data for part of each character that is [vertical 2 dots] × [horizontal 8 dots] is stored at addresses $1200M_{16}$ to $122FM_{16}$ (where M = 0, 2, 4, 6, 8, A, C, E), and data for part of each character that is [vertical 2 dots] × [horizontal 8 dots] is stored at $1200N_{16}$ to $122FN_{16}$ (where N = 1, 3, 5, 7, 9, B, D, F), as shown in Figure 57.

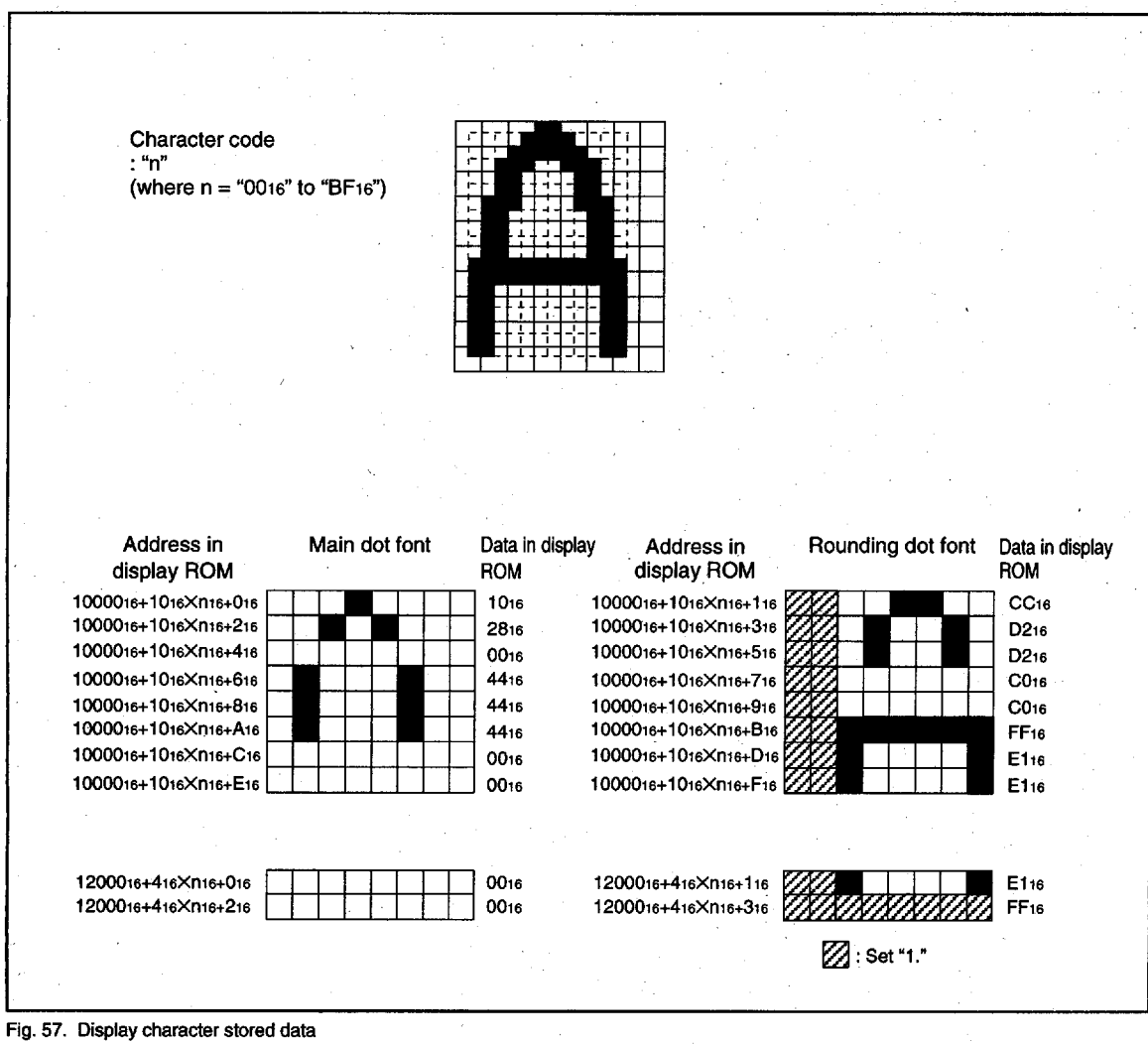


Fig. 57. Display character stored data

Table 9. Character code list (partially abbreviated)

Character code	Character data storage address			
	Main dots		Rounding dots	
	Upper 8 dots	Lower 2 dots	Upper 8 dots	Lower 2 dots
00_{16}	1000_{16}	1200_{16}	1001_{16}	1201_{16}
	1002_{16}	1202_{16}	1003_{16}	1203_{16}
	1004_{16}		1005_{16}	
	1006_{16}		1007_{16}	
	1008_{16}		1009_{16}	
	$1000A_{16}$		$1000B_{16}$	
	$1000C_{16}$		$1000D_{16}$	
	$1000E_{16}$		$1000F_{16}$	
01_{16}	1001_{16}	1204_{16}	1001_{16}	1205_{16}
	1001_{16}	1206_{16}	1001_{16}	1207_{16}
	1001_{16}		1001_{16}	
	1001_{16}		1001_{16}	
	1001_{16}		1001_{16}	
	$1001A_{16}$		$1001B_{16}$	
	$1001C_{16}$		$1001D_{16}$	
	$1001E_{16}$		$1001F_{16}$	
:	:	:	:	:
BF_{16}	$10BF_{16}$	$122FC_{16}$	$10BF_{16}$	$122FD_{16}$
	$10BF_{16}$	$122FE_{16}$	$10BF_{16}$	$122FF_{16}$
	$10BF_{16}$		$10BF_{16}$	
	$10BF_{16}$		$10BF_{16}$	
	$10BF_{16}$		$10BF_{16}$	
	$10BFA_{16}$		$10BFB_{16}$	
	$10BFC_{16}$		$10BFD_{16}$	
	$10BFE_{16}$		$10BFF_{16}$	

② RAM for display (addresses $0E00_{16}$ to $0FE1_{16}$)

The CRT display RAM is allocated at addresses $0E00_{16}$ to $0FE1_{16}$, and is divided into a display character code specification part and display attribute code part for each block. Table 10 shows the contents of the CRT display RAM.

For example, to display 1 character position (the left edge) in block 1, write the character code in address $0E00_{16}$ and write the attribute code to address $0F00_{16}$. For details on the attribute code, refer to (7) Attribute code. The structure of the CRT display RAM is shown in Figure 58.

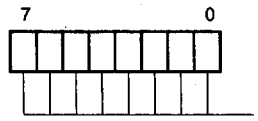
Table 10. Contents of CRT display RAM

Block	Display position (from left)	Character code specification	Attribute code specification
Block 1	1st character	$0E00_{16}$	$0F00_{16}$
	2nd character	$0E01_{16}$	$0F01_{16}$
	3rd character	$0E02_{16}$	$0F02_{16}$
	:	:	:
	32nd character	$0E1F_{16}$	$0F1F_{16}$
	33rd character	$0E20_{16}$	$0F20_{16}$
	34th character	$0E21_{16}$	$0F21_{16}$
Not used		$0E22_{16}$ to $0E3F_{16}$	$0F22_{16}$ to $0F3F_{16}$
Block 2	1st character	$0E40_{16}$	$0F40_{16}$
	2nd character	$0E41_{16}$	$0F41_{16}$
	3rd character	$0E42_{16}$	$0F42_{16}$
	:	:	:
	32nd character	$0E5F_{16}$	$0F5F_{16}$
	33rd character	$0E60_{16}$	$0F60_{16}$
	34th character	$0E61_{16}$	$0F61_{16}$
Not used		$0E62_{16}$ to $0E7F_{16}$	$0F62_{16}$ to $0F7F_{16}$
Block 3	1st character	$0E80_{16}$	$0F80_{16}$
	2nd character	$0E81_{16}$	$0F81_{16}$
	3rd character	$0E82_{16}$	$0F82_{16}$
	:	:	:
	32nd character	$0E9F_{16}$	$0F9F_{16}$
	33rd character	$0EA0_{16}$	$0FA0_{16}$
	34th character	$0EA1_{16}$	$0FA1_{16}$
Not used		$0EA2_{16}$ to $0EBF_{16}$	$0FA2_{16}$ to $0FBF_{16}$
Block 4	1st character	$0EC0_{16}$	$0FC0_{16}$
	2nd character	$0EC1_{16}$	$0FC1_{16}$
	3rd character	$0EC2_{16}$	$0FC2_{16}$
	:	:	:
	32nd character	$0EDF_{16}$	$0FDF_{16}$
	33rd character	$0EE0_{16}$	$0FE0_{16}$
	34th character	$0EE1_{16}$	$0FE1_{16}$

Blocks 1, 2, 3, 4

[Character specification]

1st character : $0E00_{16}$
to
34th character : $0E21_{16}$



Character code
Specify 192 characters ("00_{16}" to "BF_{16}")

(Block 2 ; addresses $0E40_{16}$ to $0E61_{16}$, block3 ; addresses $0E80_{16}$ to $0EA1_{16}$, block4 ; addresses $0EC0_{16}$ to $0EE1_{16}$)

[Attribute code specification]

1st character : $0F00_{16}$
to
34th character : $0F21_{16}$

Attribute code
R pin output
G pin output
B pin output
OUT1 pin output
Flash output
Underline output
Italic output
OUT2 pin output

(Block 2 ; addresses $0F40_{16}$ to $0F61_{16}$, block3 ; addresses $0F80_{16}$ to $0FA1_{16}$, block4 ; addresses $0FC0_{16}$ to $0FE1_{16}$)

Fig. 58. Structure of CRT display RAM

(7) Attribute Code

Regarding display colors, three color outputs, R, G and B, are turned on and off by controlling of the low-order 3 bits of the attribute code to display 8 color types for each character. This attribute code can be set for each character, so 7 colors can be displayed.

Whether the OUT1 pin outputs or not is switched by bit 3 of the attribute code. When the OUT1 pin outputs, which of the character output or character area OUT1 blank output is switched for each block by the OUT control register (address 0210_{16}) (refer to Figure 59). However, when the solid space auto-generating function is turned on, the character area blank output may be selected regardless of the above bit. For the solid space auto-generating function, refer to (9) Automatic Solid Space Function.

Whether OUT2 pin outputs or not is switched by bit 7 of the attribute code. When the OUT2 pin outputs, the same waveform as the character area OUT1 blank output is output.

Bits 4 to 6 of the attribute code control turning on and off flash, underline and italic respectively. Figure 60 shows an example of italic and underline display in the case where "A" is displayed with 7 × 9 dots.

Italic is formed by slanting the font stored in the display ROM to the upper right. As shown in Figure 60 (c) and (d), when italic is specified, the font overlaps in the right-adjacent character area. In the overlapped area, the display color of the left-hand character has priority. The 1st character and 34th character of each block cannot be displayed in italic.

For flash, the flash period can be changed by bit 6 of the OUT control register. However, in the flashing status, the duty is fixed at 75%. The on/off of OUT1 and OUT2 flash can be selected by bits 4 and 5, respectively.

An underline is output at the 12th dot in the vertical direction in the CCD mode. Underline specified only in the CCD mode.

Flash and italic can be specified in both modes.

Figure 61 shows the structure of the attribute code and Figure 62 shows the structure of the OUT control register.

	Bit3 of attribute code	Bits 0 to 3 of OUT control register	Function	Output example (between A and A')
(1)	0	×	No OUT1 output	R, G, B / OUT1
(2)	1	0	OUT1 output Character output	R, G, B / OUT1
(3)	1	1	OUT1 output Character area OUT1 blank output	R, G, B / OUT1

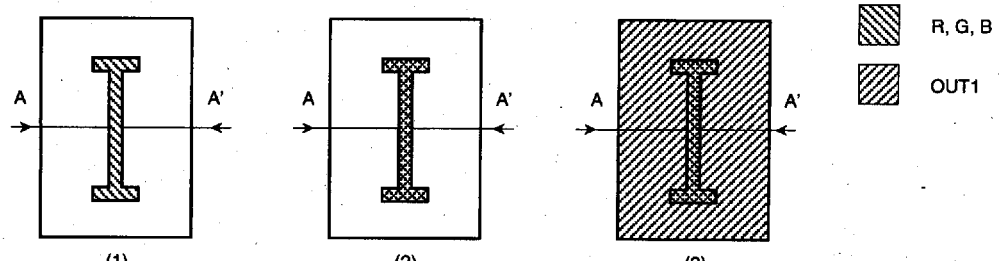


Fig. 59 Switch between character output and character area blank output

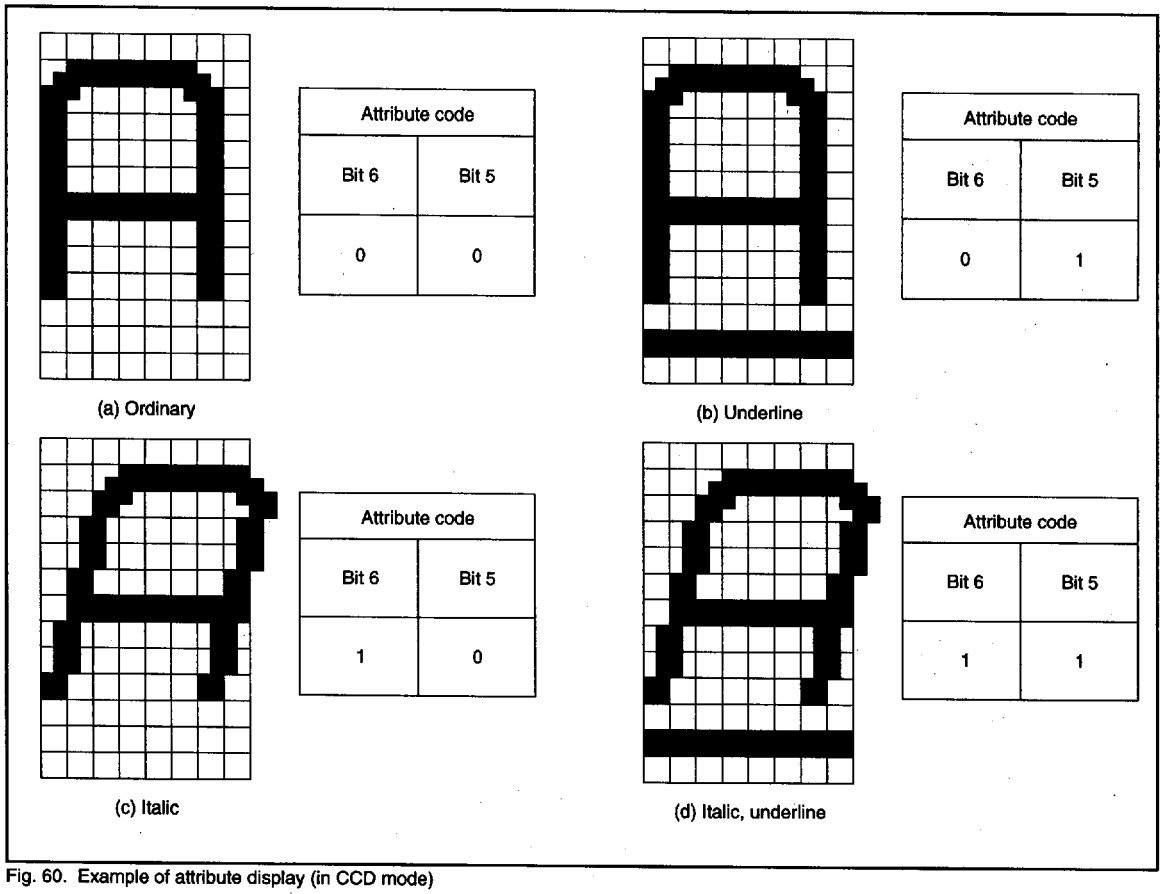


Fig. 60. Example of attribute display (in CCD mode)

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
M37267EE-XXXSP, M37267EESP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

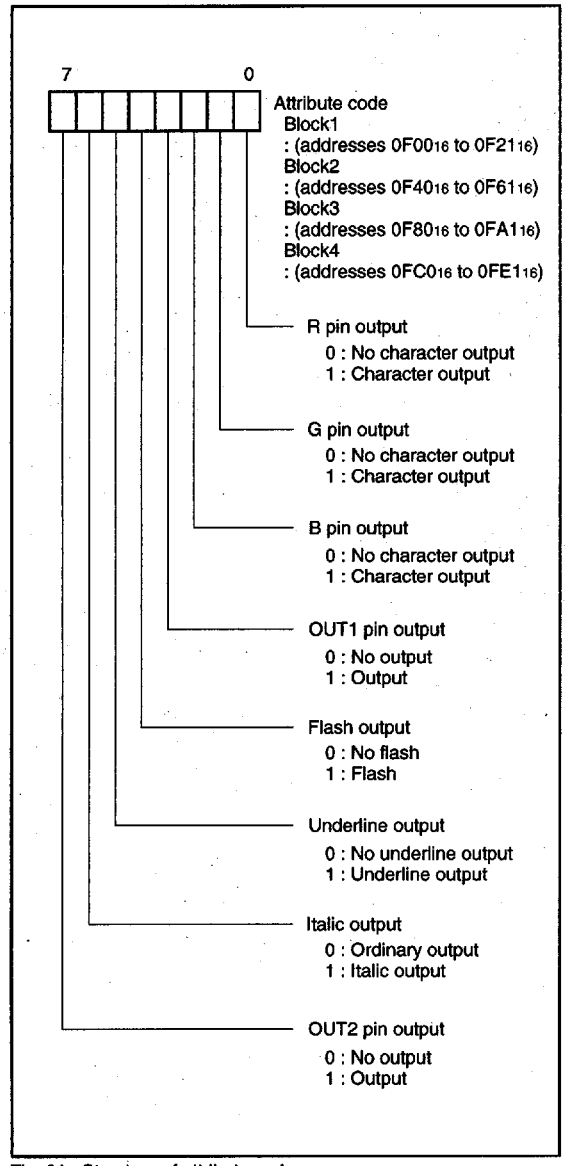


Fig. 61. Structure of attribute code

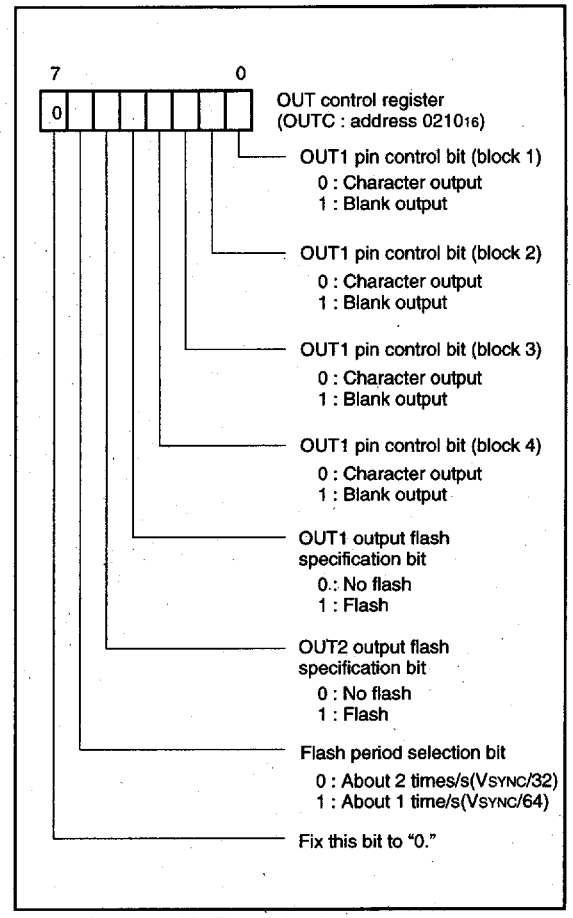


Fig. 62. Structure of OUT control register

When italic is specified as the attribute code, the blank output area, background colored area and flash (on/off) area vary depending on the display mode. In the OSD mode, if italic is specified for a character, all switch timing of the blank output, background color and flash for the character on the right side of this character becomes italic display format.

In the CCD mode, even if italic is specified, all switch timing of the blank output, background color and flash does not become an italic display format but may remain in ordinary font. The following table shows an example of the case where the character "B" is displayed in blue and the background is displayed in red. Figure 63 shows an example of combined display of italic font and ordinary font.

Table 11. Italic display correspondence table

	CCD mode		OSD mode	
	8 dots, 13 dots		8 dots, 10 dots	
	OUT1 control			Set bit 3 of attribute code to "1"
	Character output	Blank output	Character output	Blank output
	OUT1 output area, Blue	Black, Blue	Blue	Black, Blue
	Video signal and character color (blue) are not mixed.	Video signal is not displayed in blank area.	Video signal and character color (blue) are not mixed.	Video signal is not displayed in blank area.
Background color	Red, Blue	Red, Blue	Red, Blue	Red, Blue
	TV image is displayed on the character background.	TV image of character background is not displayed.	TV image is displayed on the character background.	TV image of character background is not displayed.
Color switching	This function is not available.	Blue, Red	This function is not available.	Blue, Red
		TV image of character background is not displayed.		TV image of character background is not displayed.
Flash		Blank flash area, Character flashing area		

Notes 1: The portion "B" in which character dots are displayed is not mixed with any TV video signal.
2: The wavy-lined arrows in the Table denote video signals.
3: For background color and color switching, refer to (10) Character background coloring function.

Table 11. Italic display correspondence table (continued)

	CCD mode		OSD mode	
	OUT2 control			Set bit 7 of attribute code to "1"
	OUT1 = Character output	OUT1 = Blank output	OUT1 = Character output	OUT1 = Blank output
	OUT2 output area, Blue TV image is displayed on the character background.	Black (OUT2 output area), Blue Video signal is not displayed in blank area.	OUT2 output area, Blue TV image is displayed on the character background.	Black (OUT2 output area), Blue Video signal is not displayed in blank area.
Flash		Blank flash area, Character flashing area		

Notes 1: The portion "B" in which character dots are displayed is not mixed with any TV video signal.
2: The wavy-lined arrows in the Table denote video signals.

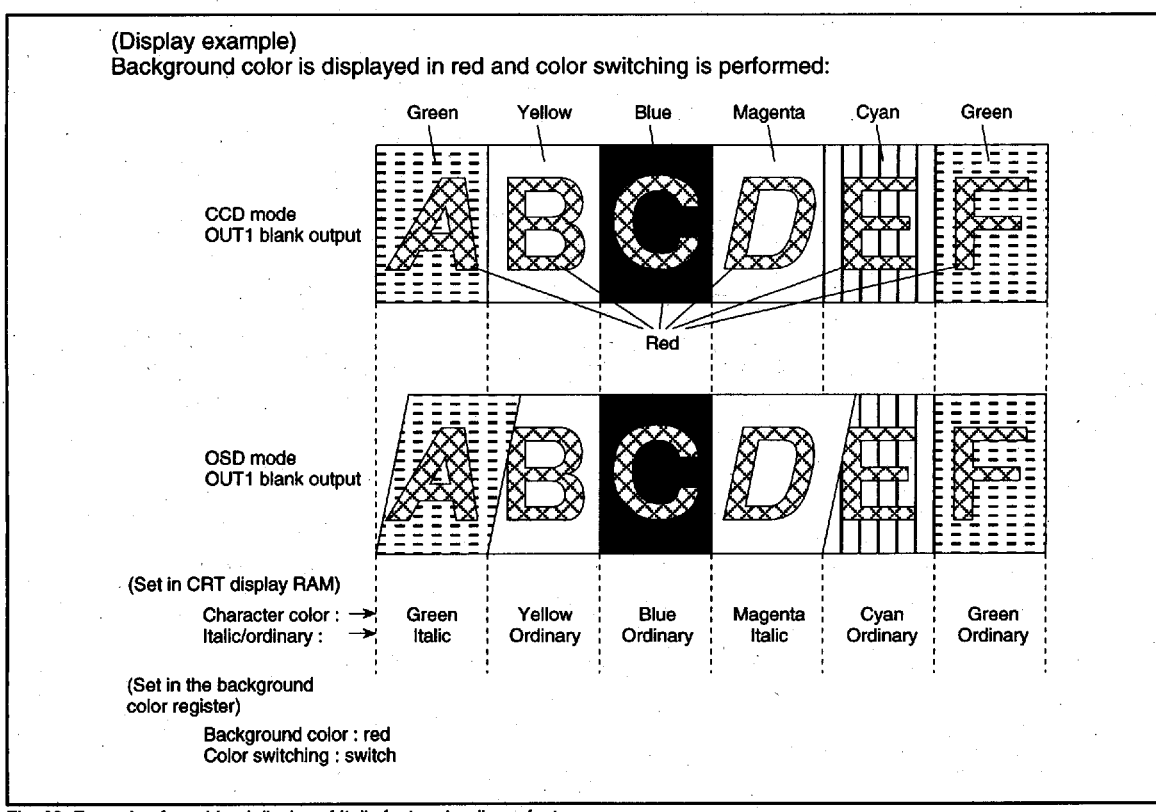


Fig. 63 Example of combined display of Italic font and ordinary font

(8) Multiline Display

The M37267M6-XXXSP can ordinarily display 4 lines on the CRT screen by displaying 4 blocks at different vertical positions. In addition, it can display up to 16 lines by using CRT interrupts.

A CRT interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical position registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block.

Note: A CRT interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display with the display control bit of the CRT control register (address $00CE_{16}$), a CRT interrupt request does not occur (refer to Figure 64).

(9) Automatic Solid Space Function

This function generates automatically the solid space (OUT1 blank output) of the character area in CCD mode.

This function is turned on and off by bit 6 of the display mode register (address $00CF_{16}$). Whether or not the OUT1 blank is output to the character area is controlled by the character code. A recognition character code ("09_{16}" or "39_{16}") for auto-generating can be selected by bit 7 of the display mode register.

Accordingly, OUT 1 blank is output the following conditions:

- When bit 3 of the attribute code is set to "1" (OUT1 output).
- When the left and right character codes including the character code to be displayed are not "39_{16}" ("09_{16}").

When using this function, select "blank output" by the OUT control register.

Note: Blank output is disabled on the left side of the 1st character and on the right side of the 34th character of each block.

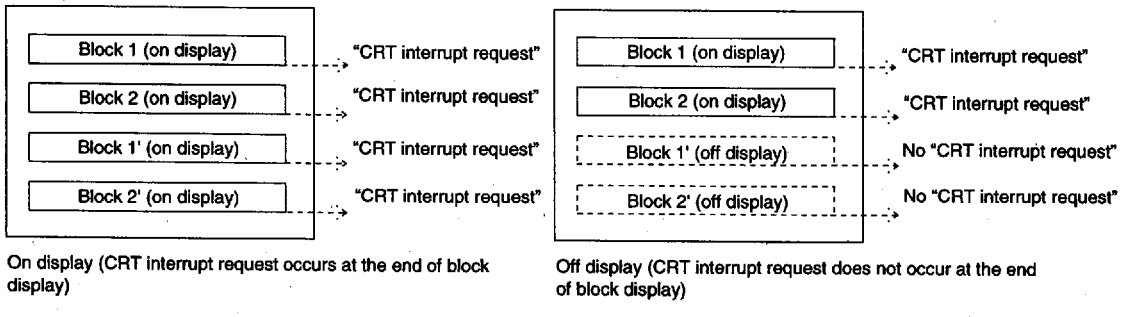


Fig. 64. Timing of CRT interrupt request

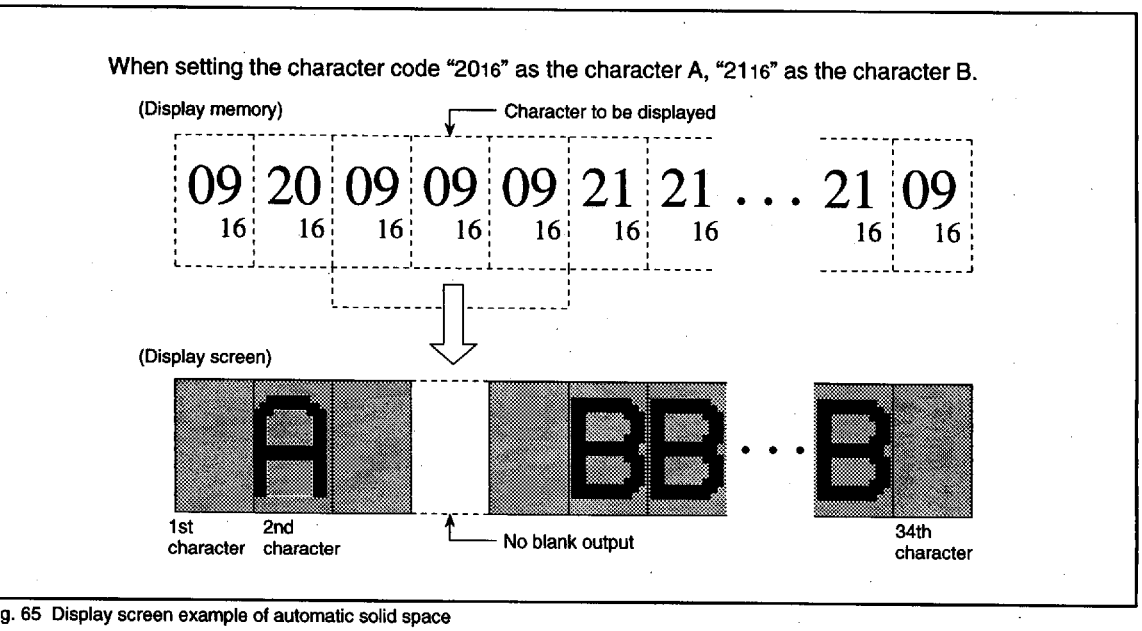


Fig. 65 Display screen example of automatic solid space

(10) Character Background Coloring Function

Character background coloring can be performed for each screen in the display area of each block. 8-color coloring is possible by setting bits 2 to 0 of the background color control register (address 00DB16). When selecting "black" for a character background color, set bits 2 to 0 each to "0."

In addition, a color switching function, which can switch between a character background color and a character color for each block, is available.

This function permits coloring for a character background color for each character. Whether or not to perform coloring switching can be controlled by bits 7 to 4 of the background color control register.

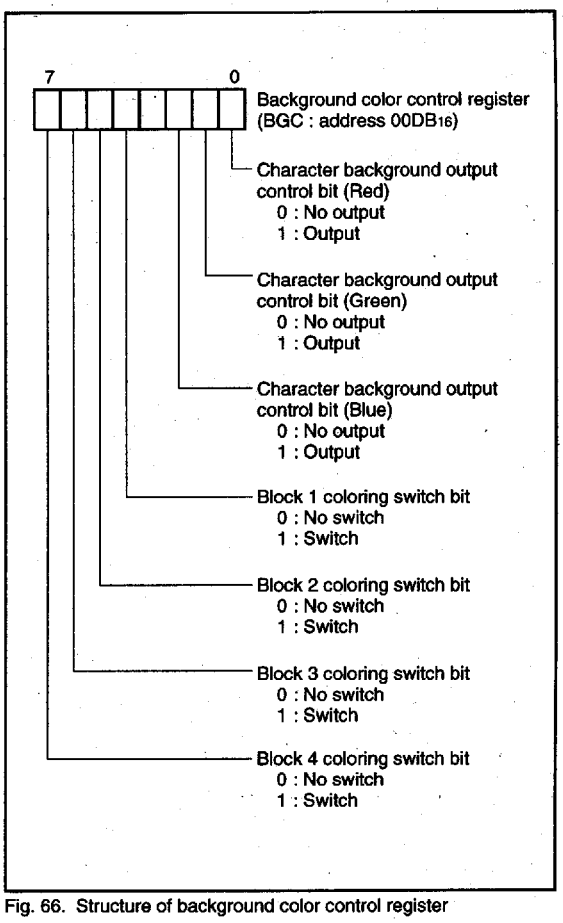
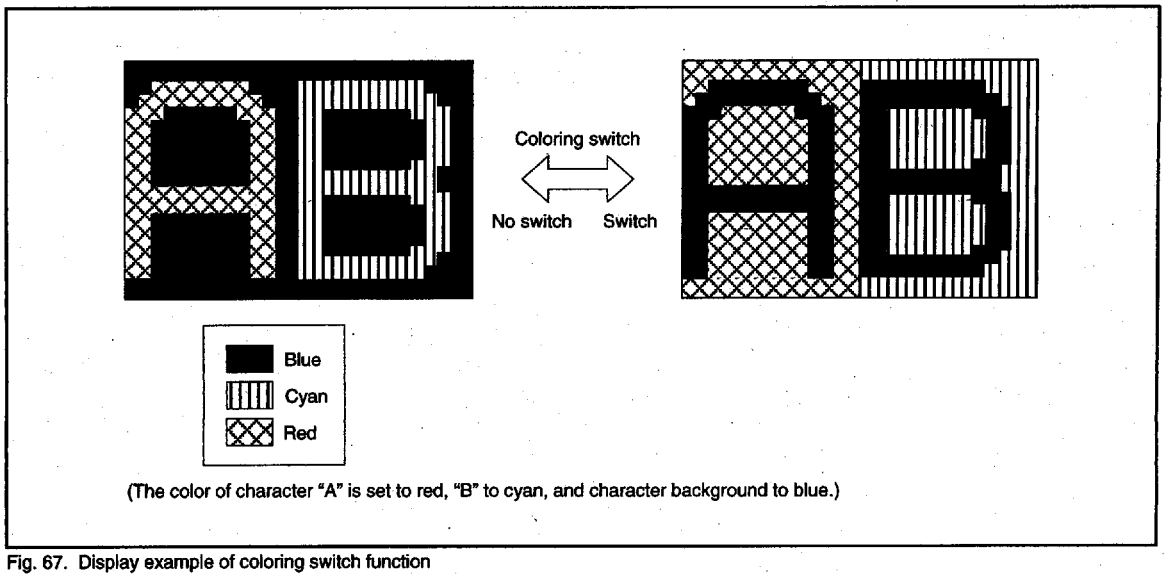


Fig. 66. Structure of background color control register



(The color of character "A" is set to red, "B" to cyan, and character background to blue.)

Fig. 67. Display example of coloring switch function

(11) Mixing Function

Color signals (MXR, MXG, MXB, and MXOUT) input from outside and color signals (R, G, B, and OUT1) generated internally can be ORed and output as a mixed signal.

The mixing control register (address 0213_{16}) can be used to turn on and off the mixing of the external and internal color signals, and also to specify which of the two signals has priority when they overlap.

The MXB and MXOUT pins can also be used as external input pins for timer 2 and timer 3.

Examples of displays generated with an internal color signal for the letter "I" and an external color signal for the letter "O" are shown in Figure 69.

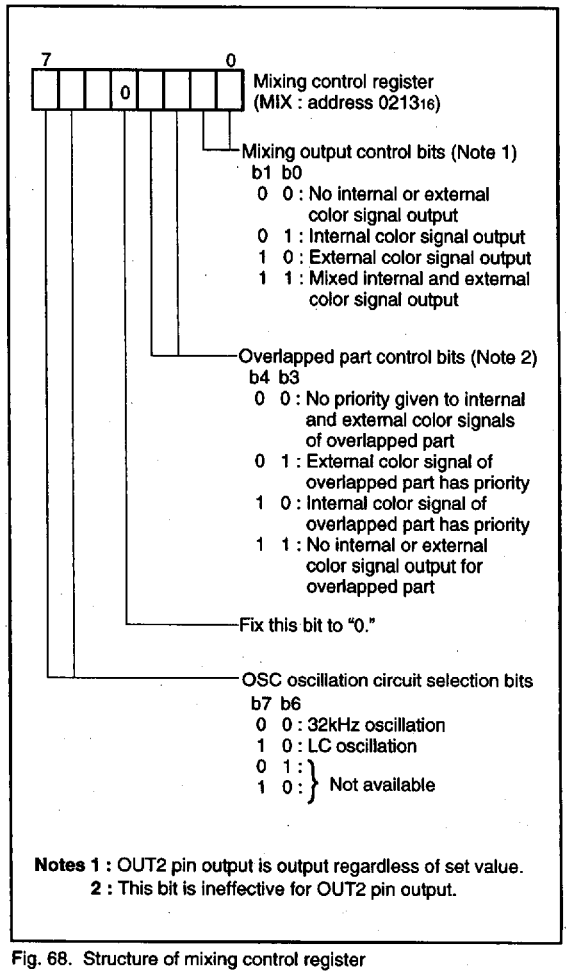
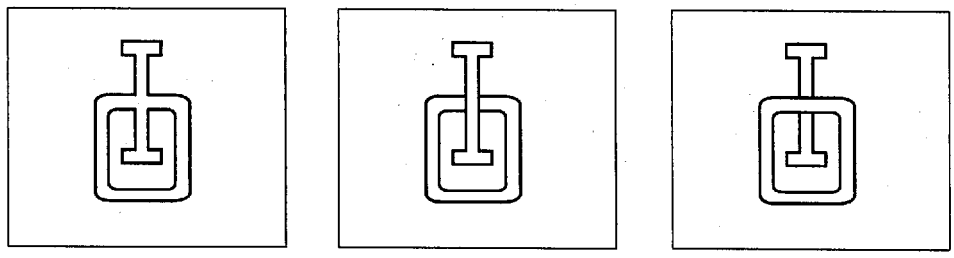


Fig. 68. Structure of mixing control register



Display when neither an external nor an internal color signal has priority

Display an internal color signal has priority

Display when an external color signal has priority

Note : The letter "I" is displayed with an internal color signal, the letter "O" is displayed with an external color signal.

Fig. 69. Example of display provided by mixing function

(12) CRT Output Pin Control

The CRT output pins R, G, B, and OUT1 can also function as ports P52, P53, P54 and P55. Set the corresponding bit of the port P5 direction register (address 00CB16) to "0" to specify these pins as CRT output pins, or set it to "1" to specify it as a general-purpose port P5 pins. The OUT2 can also function as port P10. Set bit 7 of the CRT control register (address 00CE16) to "0" to specify it as port P10, set it to "1" to specify it as OUT2 pin.

The input polarity of the HSYNC, VSYNC, MXR, MXG, MXB, and MXOUT signals can be specified with the bits of the CRT input polarity register (address 021116). The input polarity of signals HSYNC and VSYNC and output polarity of signals R, G, B, OUT1 and OUT2 can be specified with the bits of the CRT output polarity register (address 021216) . Set a bit to "0" to specify positive polarity; set it to "1" to specify negative polarity.

The structure of the CRT output polarity register is shown in Figure 70 and that of the CRT input polarity register is shown in Figure 71.

(13) Raster Coloring Function

An entire screen (raster) can be colored by setting the bits 7 to 0 of the CRT output polarity register. Since each of the R, G, B, OUT1, and OUT2 pins can be switched to raster coloring output, 7 raster colors can be obtained.

If the OUT1 pin has been set to raster coloring output, a raster coloring signal is always output during 1 horizontal scanning period. This setting is necessary for erasing a background TV image.

If the R, G, and B pins have been set to output, a raster coloring signal is output in the part except a no-raster colored character (in Figure 72, a character "O") during 1 horizontal scanning period. This ensures that character colors are not mixed with the raster color.

The raster colorling output are not mixed with the character output and with the blank output from the OUT1 pin. However, the raster coloring output is mixed with the blank output from the OUT2 pin.

An example in which a magenta character "I" and a red character "O" are displayed with blue raster coloring is shown in Figure 72.

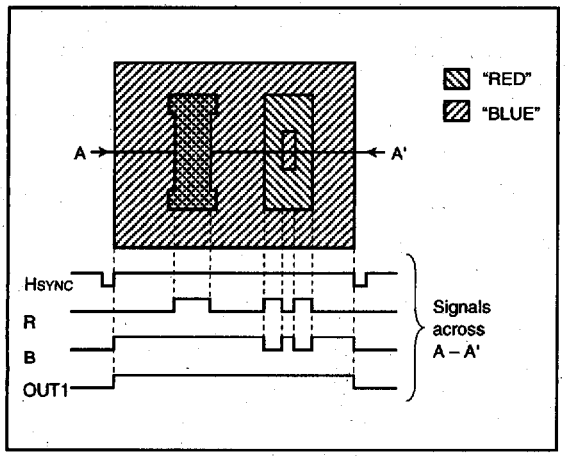


Fig. 72. Example of raster coloring

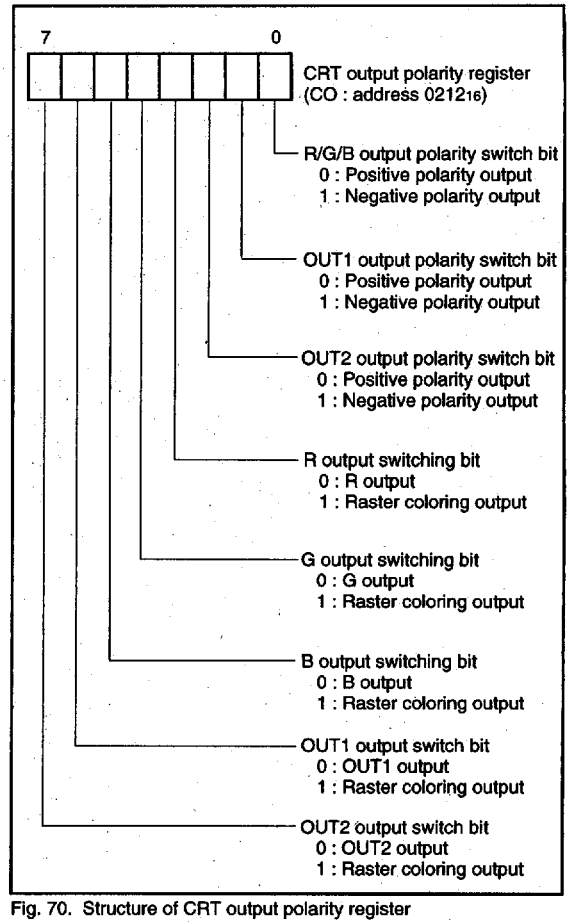


Fig. 70. Structure of CRT output polarity register

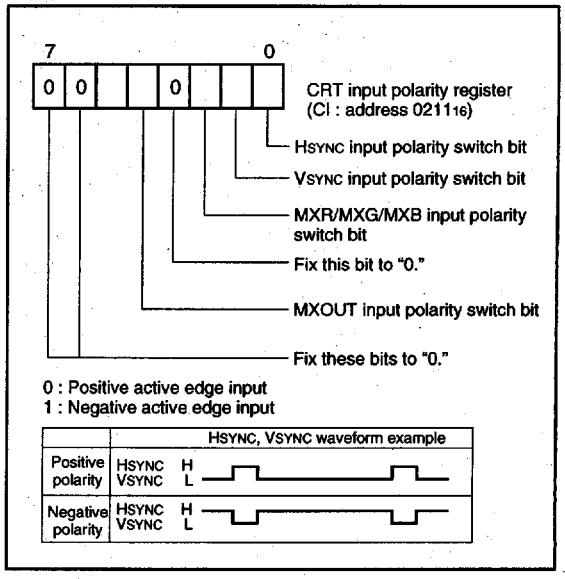


Fig. 71. Structure of CRT input polarity register

(14) Mask Function

The M37267M6-XXXSP can set a display disable area by masking the display area. However, this mask function is ineffective for the external color signals (refer to (11) Mixing Function) and the blocks with priority display (refer to (15) Priority Display Function) of raster coloring (refer to (13) Raster Coloring Function).

① Mask mode 1

In this mode, when the count value of the horizontal sync signal (HSYNC) matches the value set in the mask mode register 1, a mask is set. At the display end position of the masked block, the mask is reset. It follows that 1 display block is masked. However, when another block is displayed on the next scanning line, the mask is not reset even if the display of a masked block ends. A mask set position can be set for each line by a total of 9 bits including the mask mode register 1 (address $00DC_{16}$) and bit 4 of the vertical position register 5 (address $00D6_{16}$). When this function is not used, set the mask set position to a larger value than the number of lines of the TV set.

② Mask mode 2

This mode is started by setting bit 6 of the CRT control register (address $00CE_{16}$) to "1". In this mode, a mask is set at the timing of the vertical sync signal (VSYNC) and the mask is reset when the count value of the HSYNC signal matches the value set in the mask mode register 2 (address $00DD_{16}$). Unlike mask mode 1, the entire display up to the mask reset position is masked. This mask reset position is set by the mask mode register 2.

Fig. 74 shows a display in the case where the value of the mask mode register 2 is set in the process of block 4 and the value of the mask mode register 1 is set in the process of block 3.

A smooth Roll-up style and scrolling display in the text mode are performed by the mask function and by rewriting the value of the vertical position register with a VSYNC interrupt.

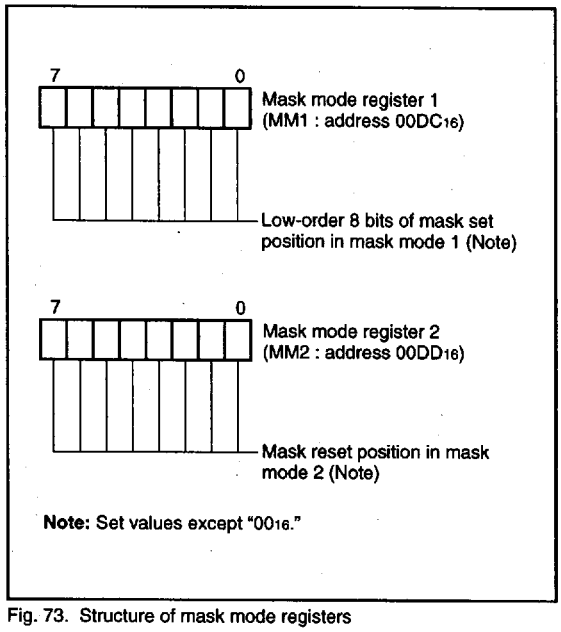
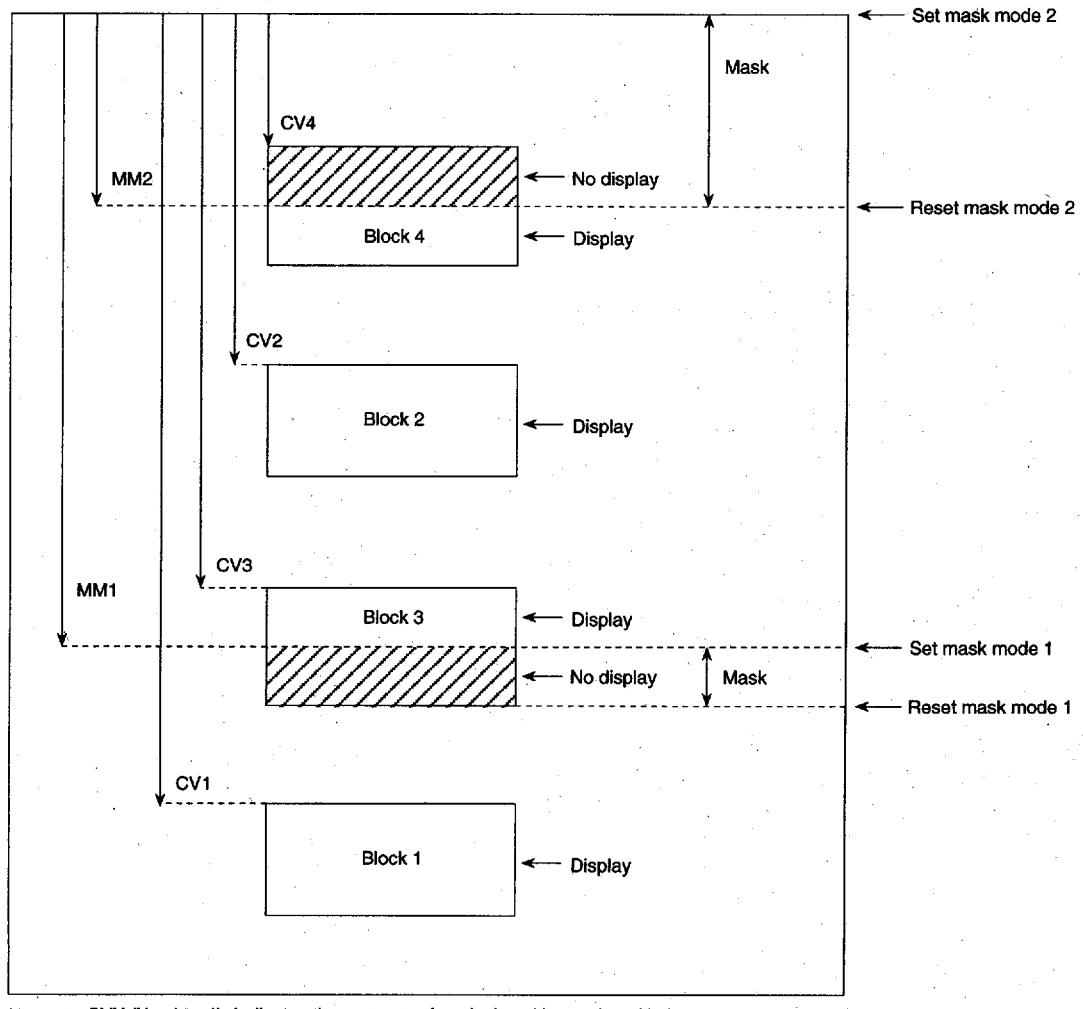


Fig. 73. Structure of mask mode registers



Notes 1: CVX (X = 1 to 4): Indicates the contents of vertical position register X.
2: MMY (Y = 1 or 2): Indicates the contents of mask mode register Y.
3: The mask function is ineffective for priority-display blocks.

Fig. 74. Mask position

(15) Priority Display Function

For blocks 1 and 2, there is a priority display function which can display these blocks with higher priority than blocks 3 and 4. This function is made effective by setting bits 1 and 0 of the priority display control register (address 00D0$_{16}$) to "1." When the vertical display start position for blocks 3 and 4 comes while blocks 1 and 2 are displayed, display of blocks 3 and 4 is not started. The blocks being displayed with priority cannot be masked.

A CRT interrupt request for blocks 1 and 2 is disabled by setting bits 2 and bit 3 of the priority display control register to "1".

Perform setting as follows by using bits 3 to 0 of the priority display control register:

①Blocks 3 and 4 are processed with multiline display by using a CRT interrupt as CCD caption display.

②Set blocks 1 and 2 to "priority display" and "no CRT interrupt request" as channel selection display. The channel selection display for a maximum of 2 lines is processed.

With the above settings of ① and ②, both caption display and channel selection control display can be simultaneously performed. When blocks 1 and 2 are set to "priority display", set the interrupt request control bit to "no CRT interrupt request."

Figure 76 shows an example of screen display using the priority display function.

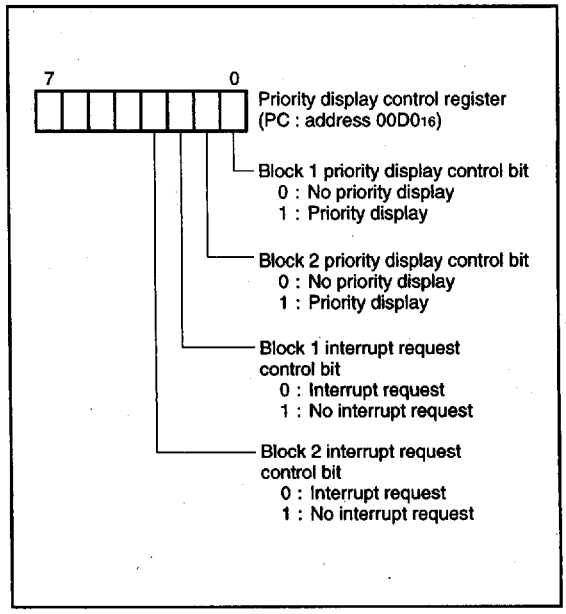


Fig. 75. Structure of priority display control register

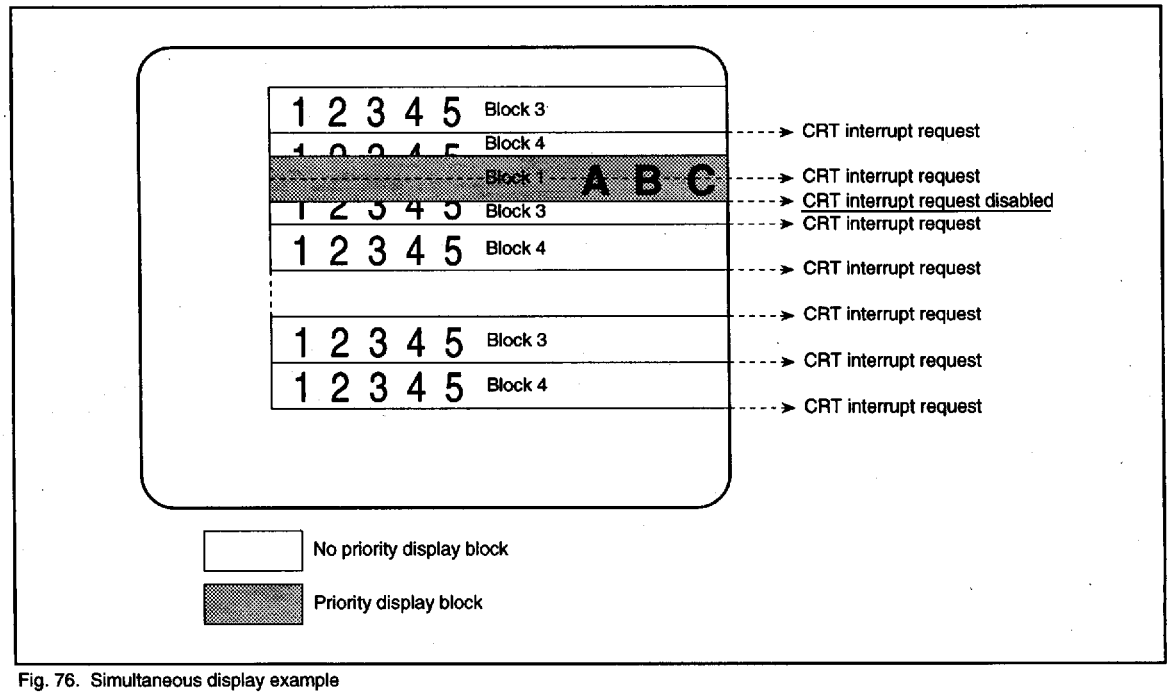


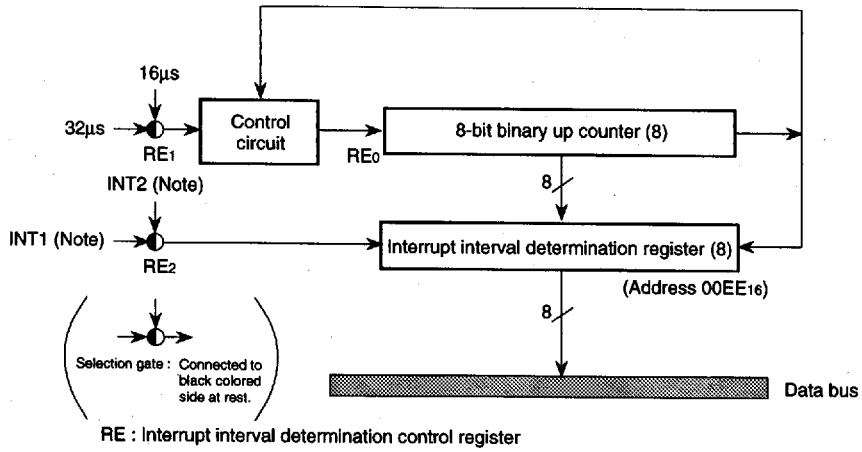
Fig. 76. Simultaneous display example

INTERRUPT INTERVAL DETERMINATION FUNCTION

The M37267M6-XXXSP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary up counter as shown in Figure 77. Using this counter, it determines an interval or a pulse width on the INT1 or INT2 (refer to Figure 79).

The following describes how the interrupt interval is determined.

1. The determination mode is selected by using bit 5 of the interrupt interval determination control register (address 00EF16). When this bit is set to "0," the interrupt interval determination mode is selected; when the bit is set to "1," the pulse width determination mode is selected.
2. The interrupt input to be determined (INT1 input or INT2 input) is selected by using bit 2 in the interrupt interval determination control register (address 00EF16). When this bit is cleared to "0," the INT1 input is selected ; when the bit is set to "1," the INT2 input is selected.
3. When the INT1 input is to be determined, the polarity is selected by using bit 3 of the interrupt interval determination control register ; when the INT2 input is to be determined, the polarity is selected by using bit 4 of the interrupt interval determination control register.
   When the relevant bit is cleared to "0," determination is made of the interval of a positive polarity (rising transition) ; when the bit is set to "1," determination is made of the interval of a negative polarity (falling transition).
4. The reference clock is selected by using bit 1 of the interrupt interval determination control register. When the bit is cleared to "0," a 32μs clock is selected ; when the bit is set to "1," a 16μs clock is selected (based on an oscillation frequency of 8MHz in either case).
5. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT1 pin (or INT2 pin), the 8-bit binary up counter starts counting up with the selected reference clock (32μs or 16μs).
6. Simultaneously with the next input pulse, the value of the 8-bit binary up counter is loaded into the interrupt interval determination register (address 00EE16) and the counter is immediately reset ("0016"). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "0016".
7. When count value "FE16" is reached, the 8-bit binary up counter stops counting. Then, simultaneously when the next reference clock is input, the counter sets value "FF16" to the interrupt interval determination register. The reference clock is generated by setting bit 0 of the PWM mode register 1 to "0."



RE : Interrupt interval determination control register

Note: The pulse width of external interrupt INT1 and INT2 needs 5 or more machine cycles.

Fig. 77. Block diagram of interrupt interval determination circuit

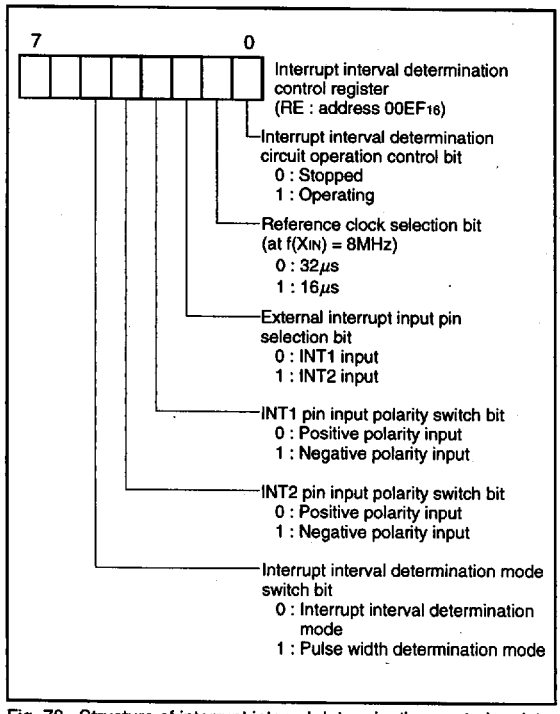


Fig. 78. Structure of interrupt interval determination control register

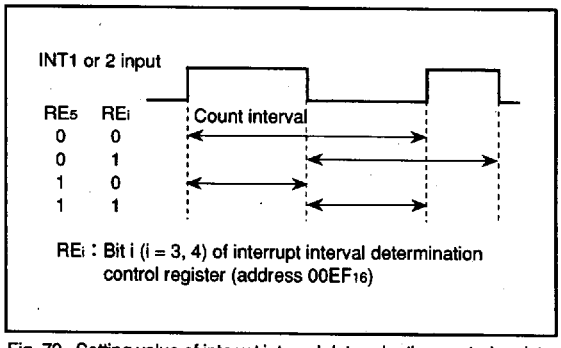


Fig. 79. Setting value of interrpt interval determination control register and measuring interval

RESET CIRCUIT

The M37267M6-XXXSP is reset according to the sequence shown in Figure 81. It starts the program from the address formed by using the content of address FFFF16 as the high-order address and the content of the address FFFE16 as the low-order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for 2 μs or more while the power source voltage is 5 V ± 10 % and the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and then returned to "H" level. The internal state of microcomputer at reset are shown in Figure 82.
An example of the reset circuit is shown in Figure 80.
The reset input voltage must be kept 0.9 V or less until the power source voltage surpasses 4.5 V.

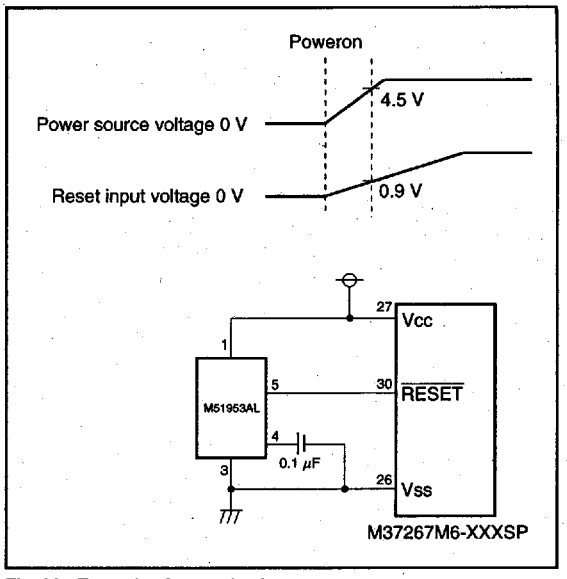


Fig. 80. Example of reset circuit

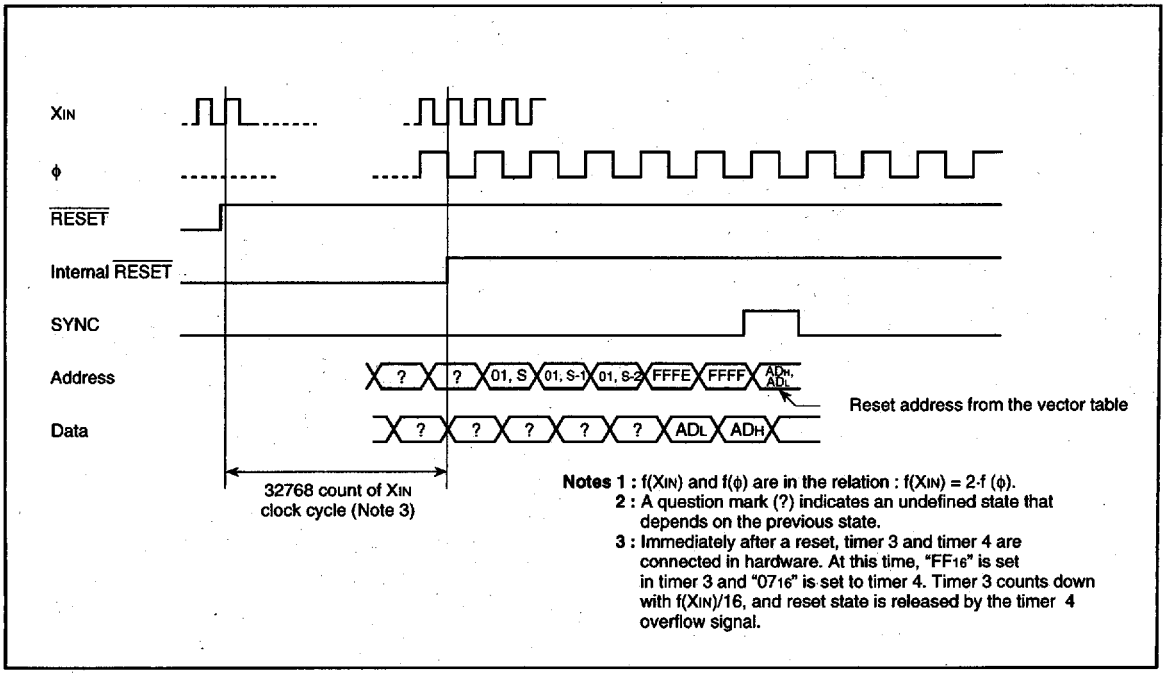


Fig. 81. Reset sequence

	Address	Contents of register
Port P0 direction register	(00C1₁₆)	00₁₆
Port P1 direction register	(00C3₁₆)	00₁₆
Port P2 direction register	(00C5₁₆)	00₁₆
Port P3 direction register	(00C7₁₆)	00₁₆
Port P4 direction register	(00C9₁₆)	00₁₆
Port P5 direction register	(00CB₁₆)	00₁₆
CRT control register	(00CE₁₆)	00₁₆
Display mode register	(00CF₁₆)	00₁₆
Priority display control register	(00D0₁₆)	⊠⊠⊠⊠0 0 0 0
Horizontal position register	(00D1₁₆)	⊠0 0 0 0 0 0 0
Vertical position register 5	(00D6₁₆)	0 0 0 * * * * *
Character size register 1	(00D7₁₆)	⊠0 0 0 ⊠0 0 0
Character size register 2	(00D8₁₆)	⊠0 0 0 ⊠0 0 0
Display clock selection register 1	(00D9₁₆)	00₁₆
Display clock selection register 2	(00DA₁₆)	00₁₆
Background color control register	(00DB₁₆)	0 0 0 0 ⊠0 0 0
Data slicer control register 1	(00DE₁₆)	00₁₆
Data slicer control register 2	(00DF₁₆)	* 0 * 0 0 * 0 0
Caption position register	(00E0₁₆)	00₁₆
Start bit position register	(00E1₁₆)	00₁₆
Window register	(00E2₁₆)	00₁₆
Sync slice register	(00E3₁₆)	00₁₆
Data register 1	(00E4₁₆)	00₁₆
Data register 2	(00E5₁₆)	00₁₆
Clock run-in register 1	(00E6₁₆)	00₁₆
Clock run-in register 2	(00E7₁₆)	00₁₆
Clockd run-in detect register 1	(00E8₁₆)	00₁₆
Clockd run-in detect register 2	(00E9₁₆)	0 0 0 0 1 0 0 1
Sync pulse counter register	(00EA₁₆)	⊠⊠0 0 0 0 0 0
Serial I/O mode register	(00EB₁₆)	00₁₆
A-D control register 1	(00ED₁₆)	0 0 1 0 0 0 0 0

	Address	Contents of register
Interrupt interval determination control register	(00EF₁₆)	⊠⊠0 0 0 0 0 0
Timer 1	(00F0₁₆)	FF₁₆
Timer 2	(00F1₁₆)	07₁₆
Timer 3	(00F2₁₆)	FF₁₆
Timer 4	(00F3₁₆)	07₁₆
Timer mode register 1	(00F4₁₆)	00₁₆
Timer mode register 2	(00F5₁₆)	00₁₆
I²C address register	(00F7₁₆)	00₁₆
I²C status register	(00F8₁₆)	0 0 0 1 0 0 0 *
I²C control register	(00F9₁₆)	00₁₆
I²C clock control register	(00FA₁₆)	00₁₆
CPU mode register	(00FB₁₆)	0 0 1 1 1 1 0 0
Interrupt request register 1	(00FC₁₆)	⊠⊠0 0 0 0 0 0
Interrupt request register 2	(00FD₁₆)	00₁₆
Interrupt control register 1	(00FE₁₆)	⊠0 0 0 0 0 0 0
Interrupt control register 2	(00FF₁₆)	00₁₆
PWM mode register 1	(020A₁₆)	⊠⊠⊠⊠0 0 0 0
PWM mode register 2	(020B₁₆)	00₁₆
Timer 5	(020C₁₆)	07₁₆
Timer 6	(020D₁₆)	FF₁₆
Timer 3 count select register	(020F₁₆)	00₁₆
OUT control register	(0210₁₆)	00₁₆
CRT input polarity register	(0211₁₆)	00₁₆
CRT output control register	(0212₁₆)	00₁₆
Mixing control register	(0213₁₆)	0 0 ⊠0 0 0 0 0
A-D control register 2	(0214₁₆)	00₁₆
Processor status register	(PS)	* * * * * 1 * *
Program counter	(PCH)	Contents of address FFFF₁₆
	(PCL)	Contents of address FFFE₁₆

Note : The contents of all other registers and RAM are undefined at reset, so set their initial values.

* : Undefined
⊠ : Unused bit

Fig. 82. Internal state of microcomputer at reset

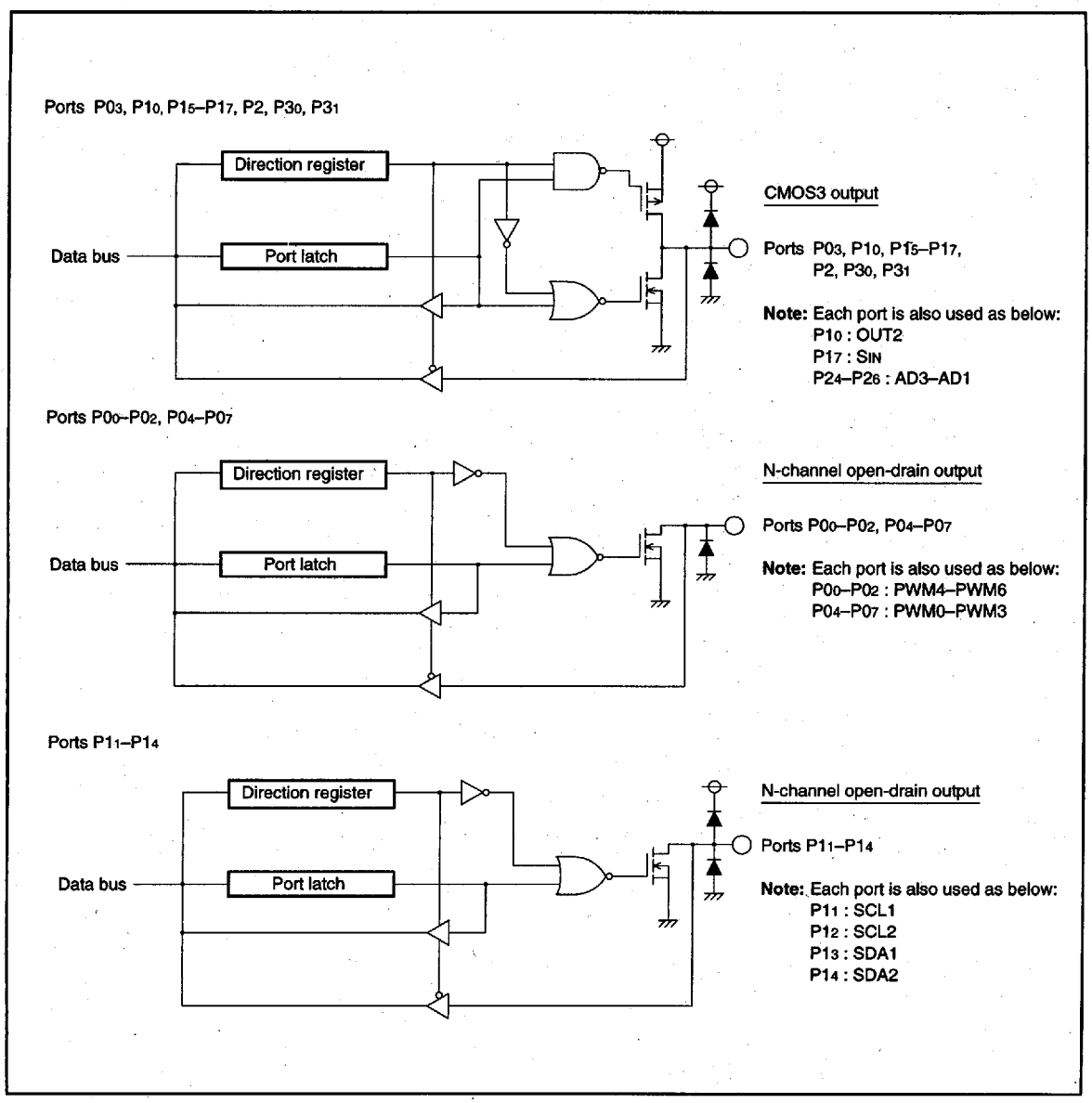


Fig. 83. I/O pin block diagram (1)

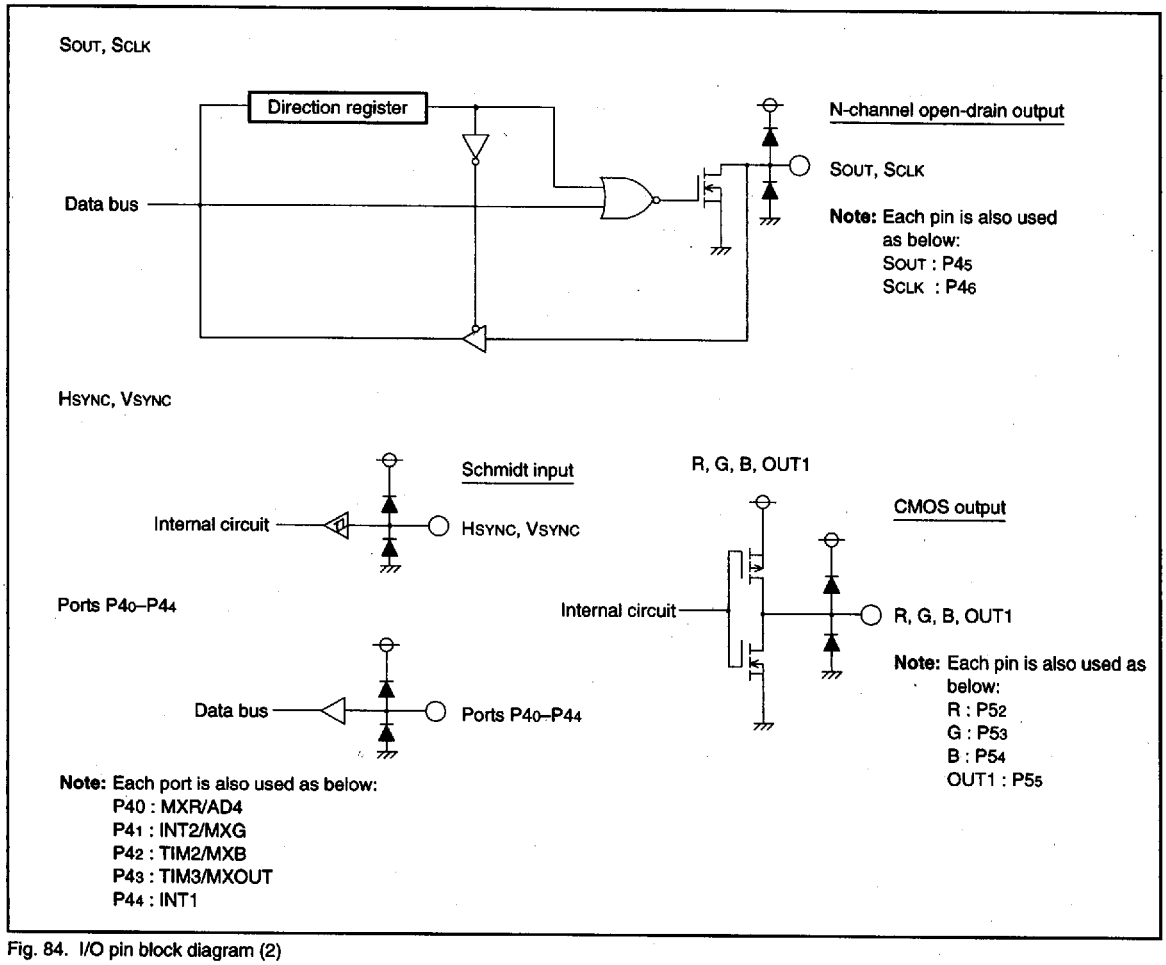


Fig. 84. I/O pin block diagram (2)

CLOCK GENERATING CIRCUIT

The M37267M6-XXXSP has 2 built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT. When using XCIN-XCOUT as sub-clock, clear bits 7 and 6 of the mixing control register to "0." To supply a clock signal externally, input it to the XIN (XCIN) pin and make the XOUT (XCOUT) pin open.

After reset has completed, the internal clock ϕ is half the frequency of XIN. Immediately after poweron, both the XIN and XCIN clock start oscillating. To set the internal clock ϕ to low-speed operation mode, set bit 7 of the CPU mode register (address 00FB16) to "1."

Oscillation Control

(1) Stop mode

The built-in clock generating circuit is shown in Figure 56. When the STP instruction is executed, the internal clock ϕ stops at "H" level. At the same time, timers 3 and 4 are connected in hardware and "FF16" is set in the timer 3, "0716" is set in the timer 4. Select f(XIN)/16 or f(XCIN)/16 as the timer 3 count source (set both bit 0 of the timer mode register 2 and bit 0 at address 020F16 to "0" before the execution of the STP instruction). And besides, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction. The oscillator restarts when external interrupt is accepted, however, the internal clock ϕ keeps its "H" level until timer 4 overflows. Because this allows time for oscillation stabilizing when a ceramic resonator or a quartz-crystal oscillator is used.

(2) Wait mode

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is released at reset or when an interrupt is accepted (Note). Since the oscillator does not stop, the next instruction can be executed at once.

Note: In the wait mode, the following interrupts are invalid.

(1) VSYNC interrupt
(2) CRT interrupt
(3) Timers 1 and 2 interrupt using P43/TIM2/MXB pin input as count source
(4) Timer 3 interrupt using P43/TIM3/MXOUT pin input as count source
(5) Data slicer interrupt
(6) Multi-master I2C-BUS interface interrupt
(7) XIN/4096 interrupt
(8) All timer interrupts using f(XIN)/2 or f(XCIN)/2 as count source
(9) All timer interrupts using f(XIN)/4096 or f(XCIN)/4096 as count source

(3) Low-Speed Mode

If the internal clock is generated from the sub-clock (XCIN), a low power consumption operation can be realized by stopping only the main clock XIN. To stop the main clock, set bit 6 (CM6) of the CPU mode register (00FB16) to "1." When the main clock XIN is restarted, the program must allow enough time to for oscillation to stabilize.

Note that in low-power-consumption mode the XCIN-XCOUT drivability can be reduced, allowing even lower power consumption (60μA with f (XCIN) = 32kHz). To reduce the XCIN-XCOUT drivability, clear bit 5 (CM5) of the CPU mode register (00FB16) to "0." At reset, this bit is set to "1" and strong drivability is selected to help the oscillation to start. When an STP instruction is executed, set this bit to "1" by software before executing.

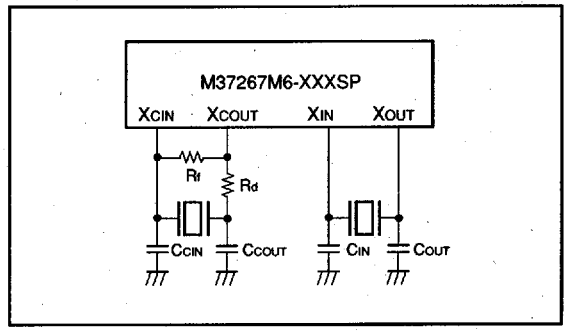


Fig. 85. Ceramic resonator circuit example

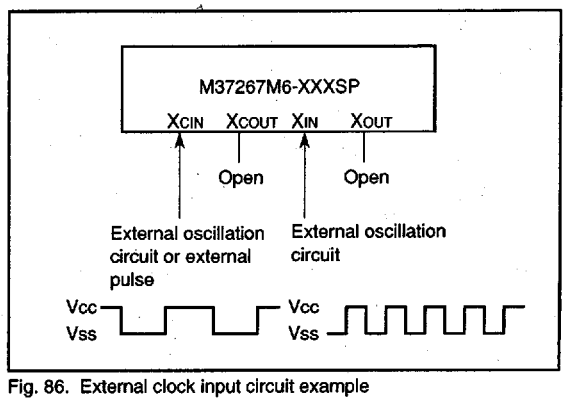
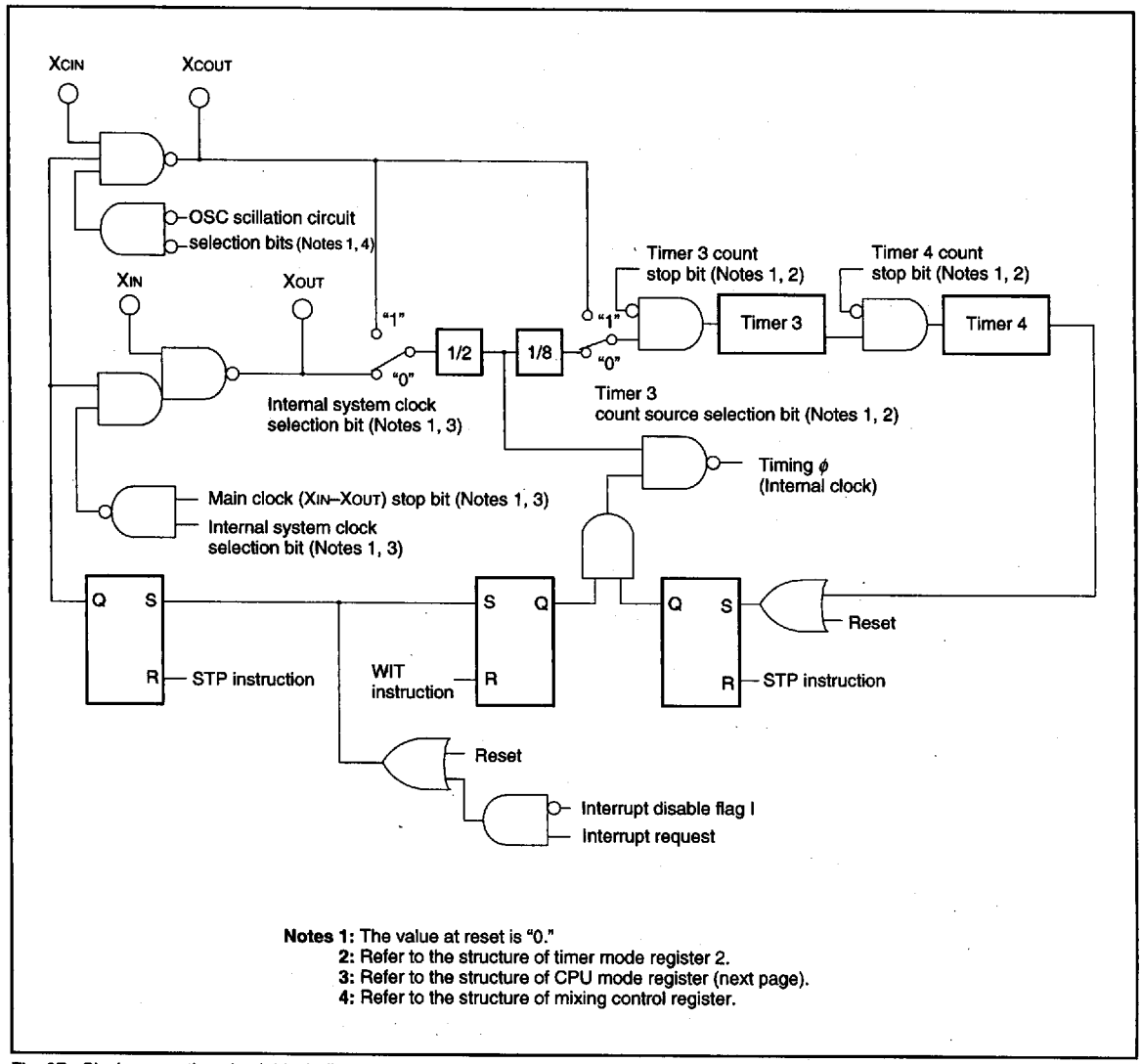
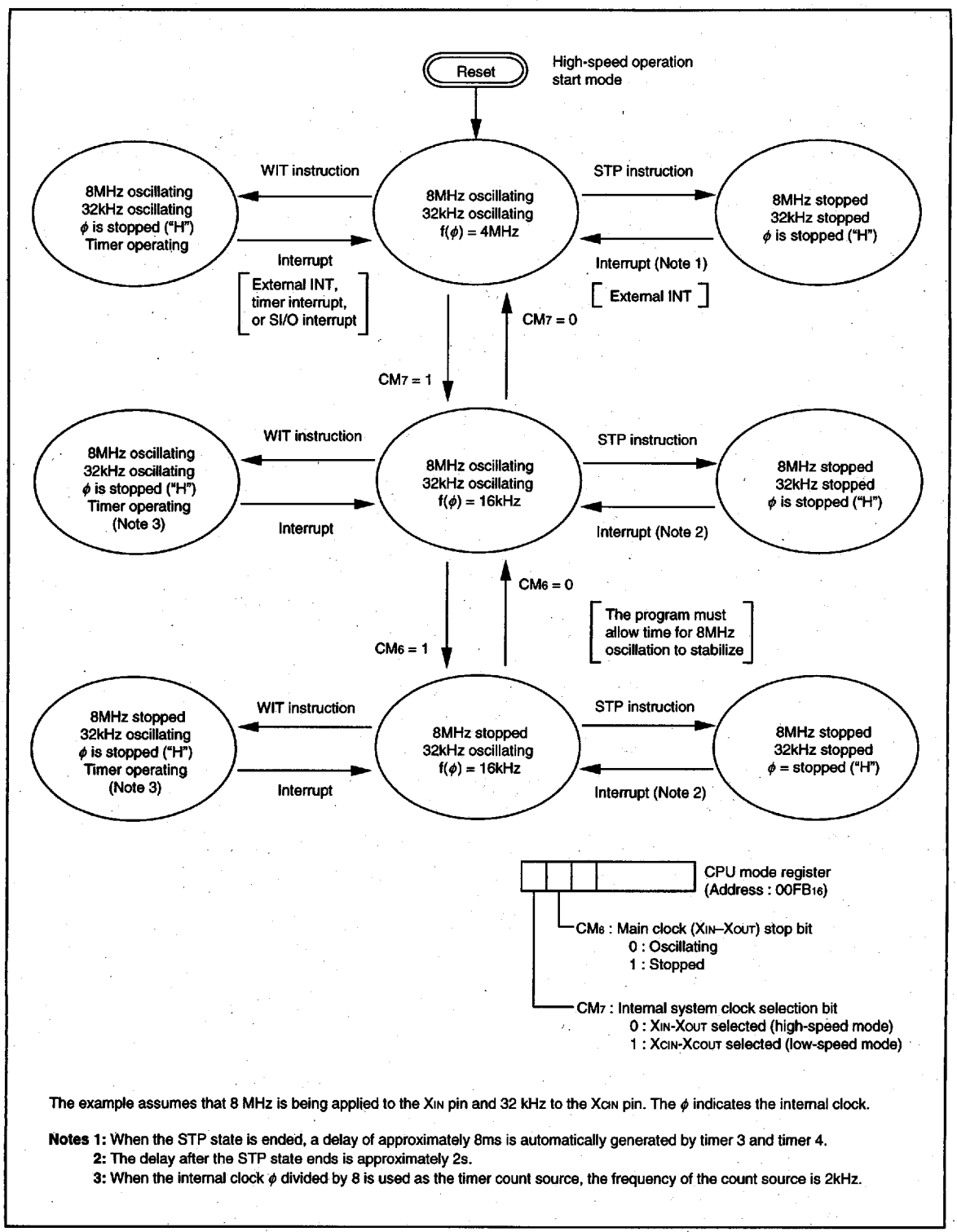


Fig. 86. External clock input circuit example



Notes 1: The value at reset is "0."
2: Refer to the structure of timer mode register 2.
3: Refer to the structure of CPU mode register (next page).
4: Refer to the structure of mixing control register.

Fig. 87. Clock generating circuit block diagram



The example assumes that 8 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. The ϕ indicates the internal clock.

Notes 1: When the STP state is ended, a delay of approximately 8ms is automatically generated by timer 3 and timer 4.
2: The delay after the STP state ends is approximately 2s.
3: When the internal clock ϕ divided by 8 is used as the timer count source, the frequency of the count source is 2kHz.

Fig. 88. State transitions of system clock

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M37267EE-XXXSP, M37267EESP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

DISPLAY OSCILLATION CIRCUIT

The CRT display clock oscillation circuit has a built-in clock oscillation circuits, so that a clock for CRT display can be obtained simply by connecting an LC across the pins OSC 1 and OSC 2. Which of the sub-clock or the display oscillation circuit is selected by setting bits 6 and 7 of the mixing control register (address 021316).

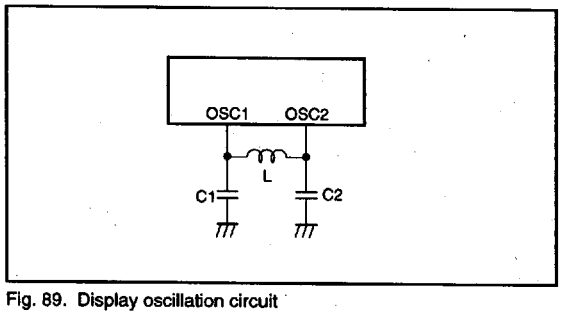
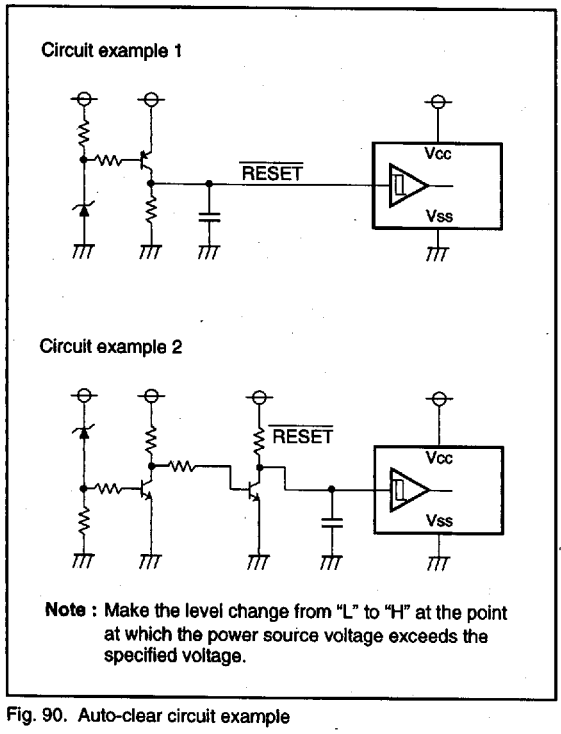


Fig. 89. Display oscillation circuit

AUTO-CLEAR CIRCUIT

When power source is supplied, the auto-clear function can be performed by connecting the following circuit to the $\overline{\text{RESET}}$ pin.



Note : Make the level change from "L" to "H" at the point at which the power source voltage exceeds the specified voltage.

Fig. 90. Auto-clear circuit example

ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to the SERIES 740 <Software> User's Manual for details.

MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to the SERIES 740 <Software> User's Manual for details.

PROGRAMMING NOTES

(1) The divide ratio of the timer is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) After the ADC and SBC instruction is executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.

(4) An NOP instruction is needed immediately after the execution of a PLP instruction.

(5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\ \mu F$) directly between the V_{CC} pin–V_{SS} pin, AV_{CC} pin–V_{SS} pin, and the V_{CC} pin–CNV_{SS} pin using a thick wire.

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M37267EE-XXXSP, M37267EESP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (28-pin DIP Type 27C101, three identical copies)

PROM Programming Method

The built-in PROM of the One Time PROM version (blank) and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37267EE	PCA7400

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 91 is recommended to verify programming.

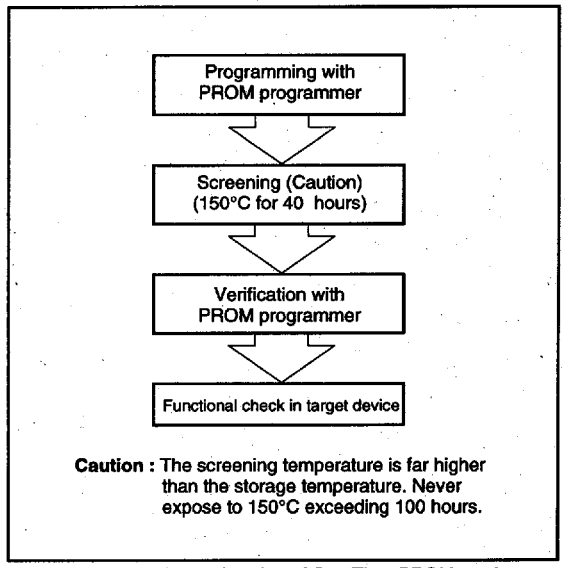

Fig. 91. Programming and testing of One Time PROM version

M37267M4-XXXSP, M37267M6-XXXSP, M37267M8-XXXSP
M37267EE-XXXSP, M37267EESP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}, AV_{CC}	Power source voltage	V_{CC}, AV_{CC}	All voltages are based on V_{SS}. Output transistors are cut off.	−0.3 to 6	V
V_I	Input voltage	CNVss		−0.3 to 6	V
V_I	Input voltage	P00–P07, P10–P17, P20–P27, P30, P31, P40–P46, P64, OSC1, XIN, HSYNC, VSYNC, RESET, CVIN		−0.3 to Vcc + 0.3	V
V_O	Output voltage	P03, P10–P17, P20–P27, P30, P31, R, G, B, OUT1, XOUT, OSC2		−0.3 to Vcc + 0.3	V
V_O	Output voltage	P00–P02, P04–P07		−0.3 to 13	V
I_{OH}	Circuit current	R, G, B, OUT1, OUT2, P03, P15–P17, P20–P27, P30, P31		0 to 1 (Note 1)	mA
I_{OL1}	Circuit current	R, G, B, OUT1, OUT2, P03, P15–P17, P20–P27, SOUT, SCLK		0 to 2 (Note 2)	mA
I_{OL2}	Circuit current	P11–P14		0 to 6 (Note 2)	mA
I_{OL3}	Circuit current	P00–P02, P04–P07		0 to 1 (Note 2)	mA
I_{OL4}	Circuit current	P30, P31		0 to 10 (Note 3)	mA
Pd	Power dissipation		Ta = 25 °C	550	mW
Topr	Operating temperature			−10 to 70	°C
Tstg	Storage temperature			−40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −10 °C to 70 °C, Vcc = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}, AV_{CC}	Power source voltage (Note 4), During CPU, CRT, data slicer operation		4.5	5.0	5.5	V
V_{CC}, AV_{CC}	RAM hold voltage (when clock is stopped)		2.0		5.5	V
V_{SS}	Power source voltage		0	0	0	V
V_{IH1}	"H" input voltage	P00–P07, P10–P17, P20–P27, P30, P31, P40–P46, P64, HSYNC, VSYNC, RESET, XIN, OSC1	0.8Vcc		Vcc	V
V_{IH2}	"H" input voltage	SCL1, SCL2, SDA1, SDA2 (When using I²C-BUS)	0.7Vcc		Vcc	V
V_{IL1}	"L" input voltage	P00–P07, P10–P17, P20–P27, P30, P31, P40–P46, P63, P64	0		0.4 Vcc	V
V_{IL2}	"L" input voltage	SCL1, SCL2, SDA1, SDA2 (When using I²C-BUS)	0		0.3 Vcc	V
V_{IL3}	"L" input voltage (Note 6)	P41–P44, P46, P17, HSYNC, VSYNC, RESET, XIN, OSC1	0		0.2 Vcc	V
I_{OH}	"H" average output current (Note 1)	R, G, B, OUT1, OUT2, P03, P15–P17, P20–P27, P30, P31			1	mA
I_{OL1}	"L" average output current (Note 2)	R, G, B, OUT1, OUT2, P03, P15–P17, P20–P27, SOUT, SCLK			2	mA
I_{OL2}	"L" average output current (Note 2)	P11–P14			6	mA
I_{OL3}	"L" average output current (Note 2)	P00–P02, P04–P07			1	mA
I_{OL4}	"L" average output current (Note 3)	P30, P31			10	mA
fCPU	Oscillation frequency (for CPU operation) (Note 5)	XIN	3.6	8.0	8.1	MHz
fCLK	Oscillation frequency (for sub-clock operation) (Note 7)		29	32	35	kHz
fCRT	Oscillation frequency (for CRT display)	OSC1	6.0		13.0	MHz
fhs1	Input frequency	TIM2, TIM3, INT1, INT2			100	kHz
fhs2	Input frequency	SCLK			1	MHz
fhs3	Input frequency	SCL1, SCL2			400	kHz
fhs4	Input frequency	Horizontal sync. signal of video signal	15.262	15.734	16.206	kHz
V_I	Input amplitude video signal	CVIN	1.5	2.0	2.5	V

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M37267EE-XXXSP, M37267EESP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with CLOSED CAPTION DECODER and ON-SCREEN DISPLAY CONTROLLER

ELECTRIC CHARACTERISTICS (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, Ta = −10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
I_{CC}	Power source current	System operation	V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz	CRT OFF Data slicer OFF		15	30	mA
				CRT ON Data slicer ON		30	45	
			V_{CC} = 5.5 V, f(X_{IN}) = 0, f(X_{CIN}) = 32kHz, CRT OFF, Data slicer OFF, Low-power dissipation mode set (CM_5 = "0", CM_6 = "1")			60	200	μA
		Wait mode	V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz			2	4	mA
			V_{CC} = 5.5 V, f(X_{IN}) = 0, f(X_{CIN}) = 32kHz, Low-power dissipation mode set (CM_5 = "0", CM_6 = "1")			25	100	μA
		Stop mode	V_{CC} = 5.5 V, f(X_{IN}) = 0, f(X_{CIN}) = 0			1	10	
V_{OH}	"H" output voltage	R, G, B, OUT1, OUT2, $P0_3$, $P15$–$P17$, $P20$–$P27$, $P30$, $P31$	V_{CC} = 4.5 V, I_{OH} = −0.5 mA		2.4			V
V_{OL}	"L" output voltage	R, G, B, OUT1, OUT2, S_{OUT}, S_{CLK}, $P00$–$P07$, $P15$–$P17$, $P20$–$P22$	V_{CC} = 4.5 V, I_{OL} = 0.5 mA				0.4	V
	"L" output voltage	$P30$, $P31$	V_{CC} = 4.5 V, I_{OL} = 0.5 mA				3.0	
	"L" output voltage	$P11$–$P14$	V_{CC} = 4.5 V	I_{OL} = 3 mA			0.4	
				I_{OL} = 6 mA			0.6	
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$	V_{CC} = 5.0 V			0.5	0.7	V
	Hysteresis (Note 6)	H_{SYNC}, V_{SYNC}, $P41$–$P44$, $P46$, $P11$–$P14$, $P17$	V_{CC} = 5.0 V			0.5	1.3	
I_{IZH}	"H" input leak current	$\overline{RESET}$, $P0_3$, $P10$–$P17$, $P20$–$P27$, $P30$, $P31$, $P40$–$P46$, $P63$, $P64$, H_{SYNC}, V_{SYNC}	V_{CC} = 5.5 V, V_I = 5.5 V				5	μA
I_{IZL}	"L" input leak current	$\overline{RESET}$, $P00$–$P07$, $P10$–$P17$, $P20$–$P27$, $P30$, $P31$, $P40$–$P46$, $P63$, $P64$, H_{SYNC}, V_{SYNC}	V_{CC} = 5.5 V, V_I = 0 V				5	μA
I_{OZH}	"H" output leak current	$P00$–$P02$, $P04$–$P07$	V_{CC} = 5.5 V, V_O = 12 V				10	μA
R_{BS}	I^2C-BUS-BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		V_{CC} = 4.5 V				130	Ω

Notes 1: The total current that flows out of the IC must be 20 mA (max.).

2: The total input current to IC (I_{OL1} + I_{OL2} + I_{OL3}) must be 20 mA or less.

3: The total average input current for ports $P30$, $P31$ to IC must be 10 mA or less.

4: Connect 0.1 μF or more capacitor externally across the power source pins V_{CC}–V_{SS} and AV_{CC}–V_{SS} so as to reduce power source noise.
Also connect 0.1 μF or more capacitor externally across the pins V_{CC}–CNVss.

5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.

6: $P41$–$P44$ have the hysteresis when these pins are used as interrupt input pins or timer input pins. $P11$–$P14$ have the hysteresis when these pins are used as multi-master I^2C-BUS interface ports. $P17$ and $P46$ have the hysteresis when these pins are used as serial I/O pins.

7: When using the sub-clock, set f_{CLK} < f_{CPU}/3.

A-D COMPARATOR CHARACTERISTICS

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, Ta = −10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				6	bits
—	Non-linearity error		0		±1	LSB
—	Differential non-linearity error		0		±1.5	LSB
V_{OT}	Zero transition error	V_{CC} = 5.12V I_{OL} (SUM) = 0mA	0		1.5	LSB
V_{FST}	Full-scale transition error	V_{CC} = 5.12V	0		−2	LSB
V_{IA}	Analog input current		0		V_{CC}	V

MULTI-MASTER I²C-BUS BUS LINE CHARACTERISTICS

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		μs
$t_{HD:STA}$	Hold time for START condition	4.0		0.6		μs
t_{LOW}	"L" period of SCL clock	4.7		1.3		μs
t_R	Rising time of both SCL and SDA signals		1000	20+0.1Cb	300	ns
$t_{HD:DAT}$	Data hold time	0		0	0.9	μs
t_{HIGH}	"H" period of SCL clock	4.0		0.6		μs
t_F	Falling time of both SCL and SDA signals		300	20+0.1Cb	300	ns
$t_{SU:DAT}$	Data set-up time	250		100		ns
$t_{SU:STA}$	Set-up time for repeated START condition	4.7		0.6		μs
$t_{SU:STO}$	Set-up time of STOP condition	4.0		0.6		μs

Note: Cb = total capacitance of 1 bus line

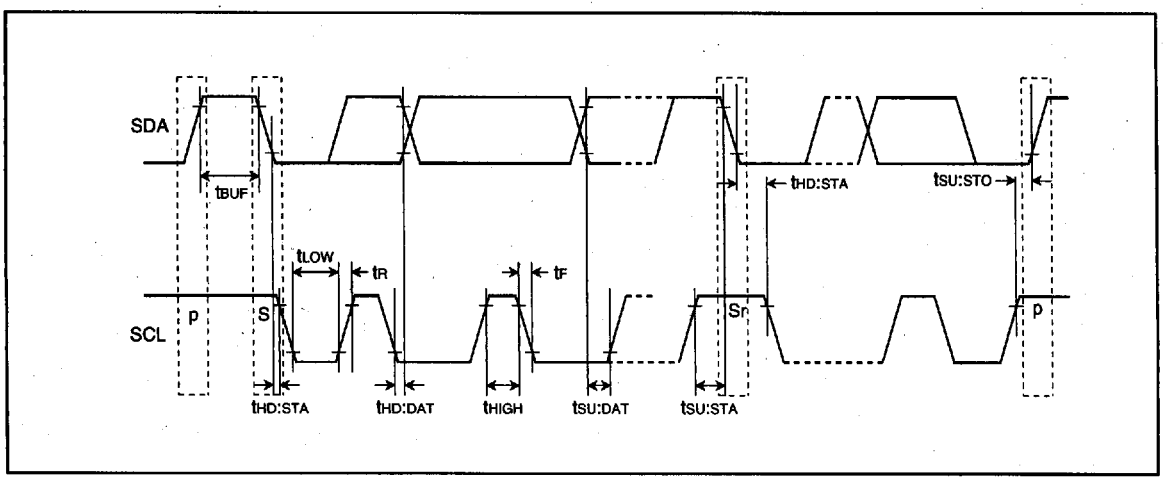

Fig. 92. Definition diagram of timing on multi-master I²C-BUS

Note 28. Self refresh sequence
Two refreshing ways should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$
1.1 Distriduted refresh during Read/Write operation
(A) Timing Diagrams

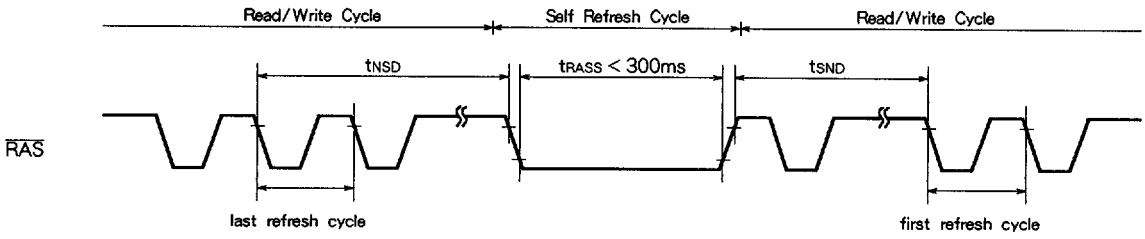

Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of refresh

Definition of CBR distributed refresh

The CBR distributed refresh performs more then 1024 discrete CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 discrete $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.1.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

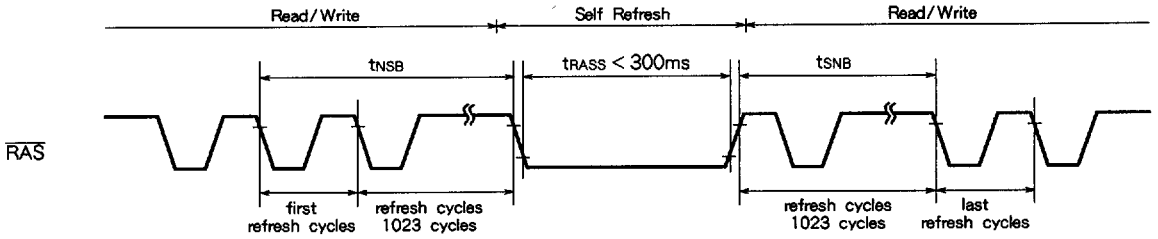

Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more then 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.2.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read /write operation period should be set within 16.4 ms.

1.2.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/ write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geqq 300ms$
(A) Timing diagram

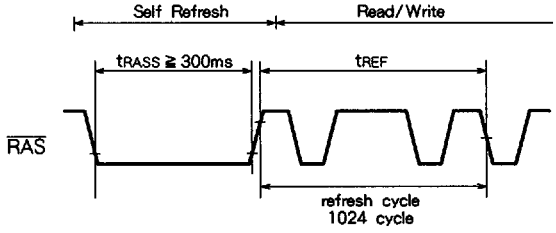

Table 4

Read/Write	Self Refresh→Read/Wirte
CBR distributed refresh $\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	$t_{REF} \leqq 16.4ms$

(B) Definition of refresh
The same as 1.1-(B) and 1.2-(B)

2.1
Regardless of the refresh (CBR distributed refresh, $\overline{RAS}$ only distributed refresh, CBR burst refresh, $\overline{RAS}$ only burst refresh) during Read/Write operation the minimum of 1024 cycles refresh should be preformed within 16.4 ms from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation.